High-Speed Data AcQuisition System Development for a new 262k Pixels X-Ray Camera at the SOLEIL Synchrotron

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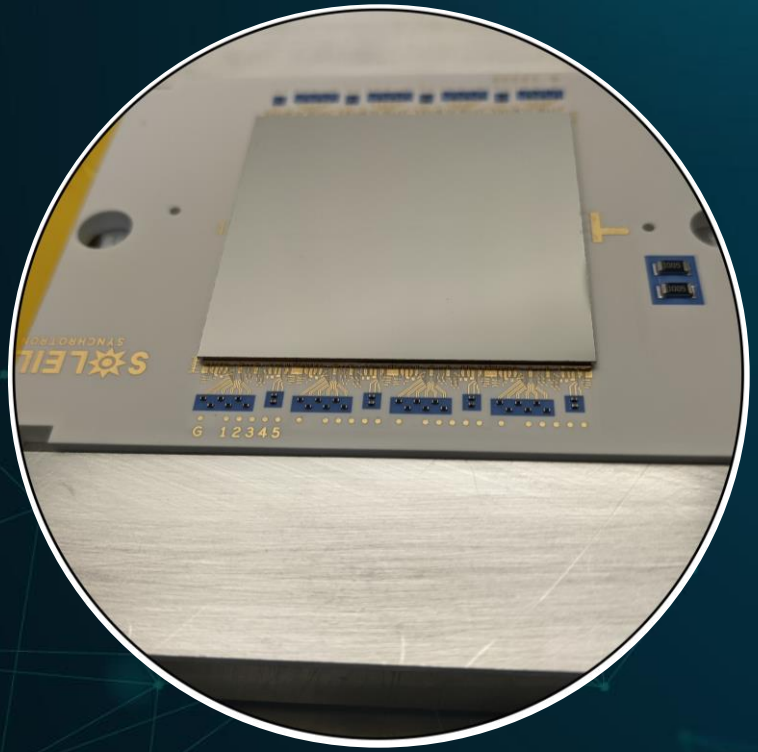


01

INTRODUCTION

1.1 Motivation

SOLEIL Synchrotron

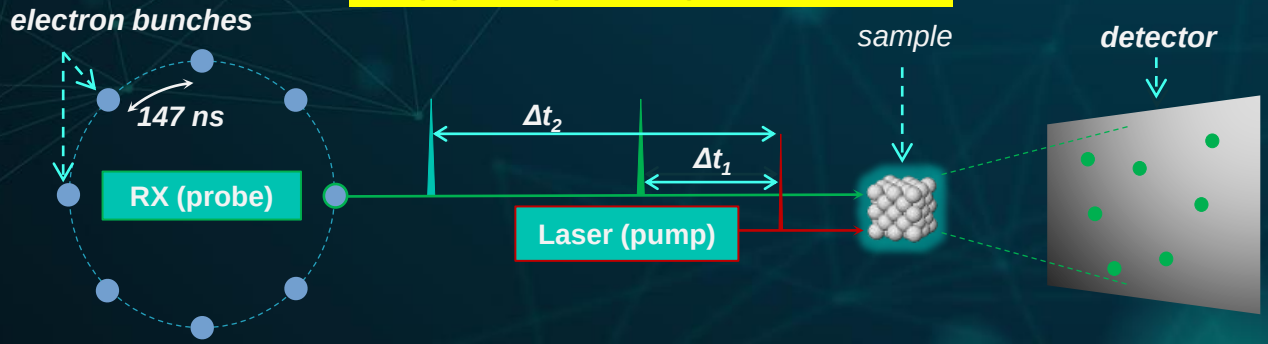
- 3rd Generation radiation source
- 29 Operational beamline with support groups
- Very large energy spectrum: 0.1 meV – 100 keV

We target applications that requires high framerate (thus high data throughput), high photons count rate ➔ diffraction, time resolved measurements (ex. pump-probe-probe) .

Challenging detector requirements

- Shutterless single bunch separation ➔ min. counting time ≈100 ns
- Synchronization with synchrotron bunches ➔ gateable
- Energy selection ➔ 2 thresholds (two images)
- 5 kHz laser repetition rated (pump) ➔ min. 20 kfps (2 images/thresholds and 2 probes)
- Single photon resolution and high dynamic range ➔ photon counting approach
- High beam flux ➔ above 10^9 ph/s/mm^2
- min. working energy 7 keV ➔ min. threshold ≈3.5 keV

Pump-probe-probe experiment scheme



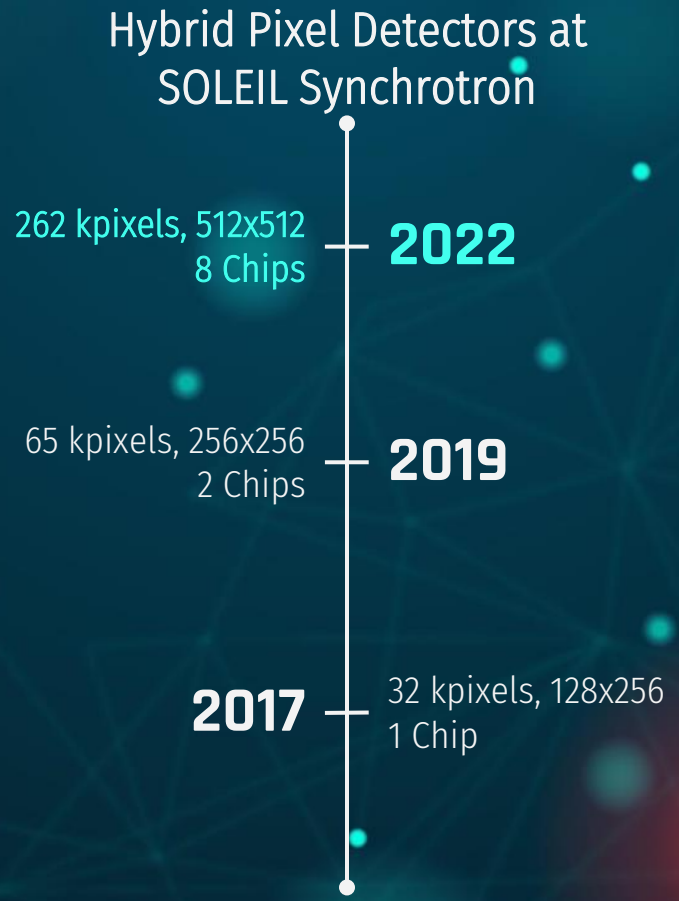
1.2 Detector characteristics

Ultra Fast X-ray Chip UFXC32k main characteristics

- Energy range up to 15 keV with 320 µm thick Si sensor
- Designed by AGH-USC (Krakow, PL)
- matrix: 128 × 256 pixels (9.6 × 20.1 mm²)
- pixel size: 75 × 75 µm²
- high framerate (> 50 kHz @ 2-bits readout)
- min. counting time <100 ns
- two discriminator, two counters (14 bits)
- high counting linearity (> 10^6 ph/pix/sec)

High-speed data transfer of 8 Chips with 50 kHz (2-bits acquisition mode) ➔ **High bandwidth is then required**

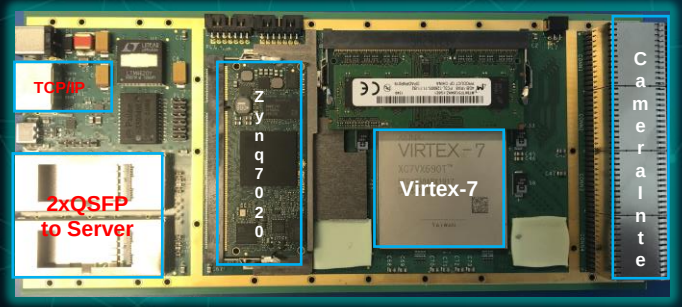
Image depth	Chip Clock DDR (MHz)	Max Image Framerate (kHz)	Bandwidth (Gb/s)
2	225	51.70	25.85
8	225	13.52	27.04
14	225	7.77	27.20



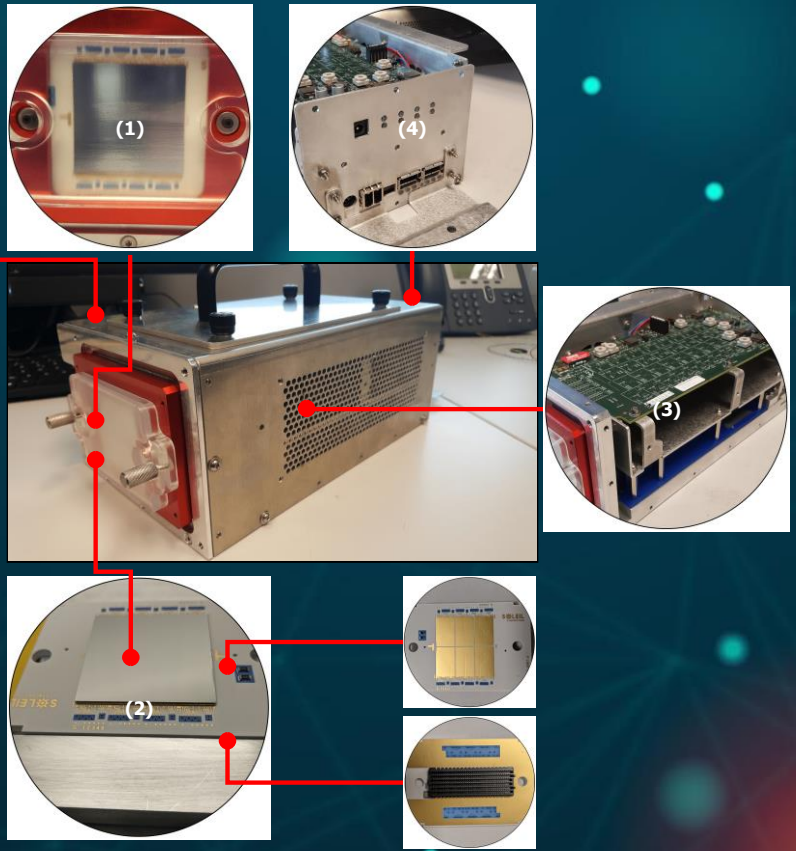
1.3 Detector Architecture

- Increased detector size to 4 × 4 cm² (2x4 chips, 513 px × 515 px)
- DAQ and DET integrated within the same body
- Increased max framerate: 50 kHz @ 2 bits / 7 kHz @ 14 bits
- Max data throughput > 24 Gbps (over 4x10 Gb links)

- (1) Camera hybrid modules
- (2) DET board
- (3) DAQ and Power boards
- (4) Camera Communication Interfaces
- (5) Cooling and housing
- (6) Adaptation board



Layout of the FEM-II DAQ board



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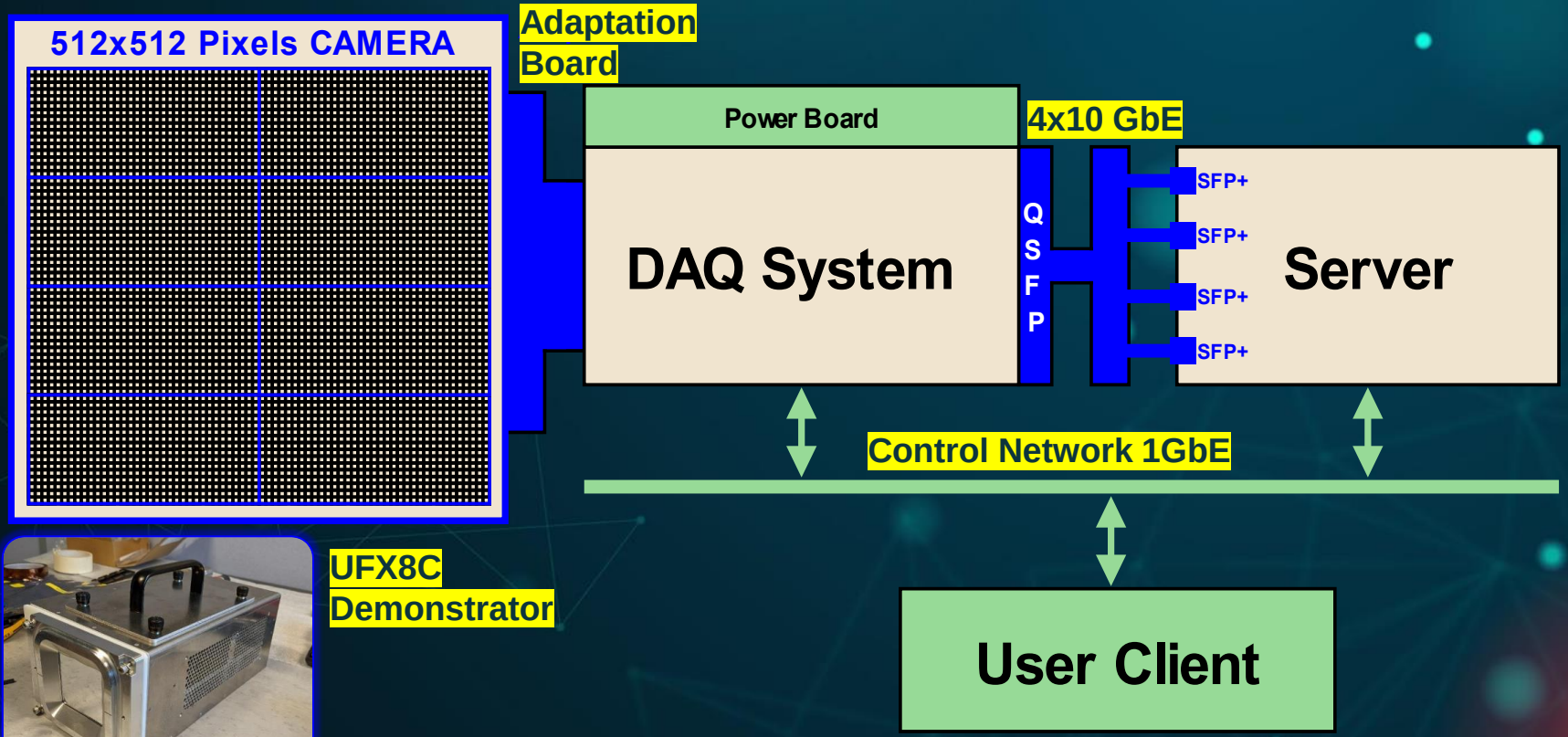
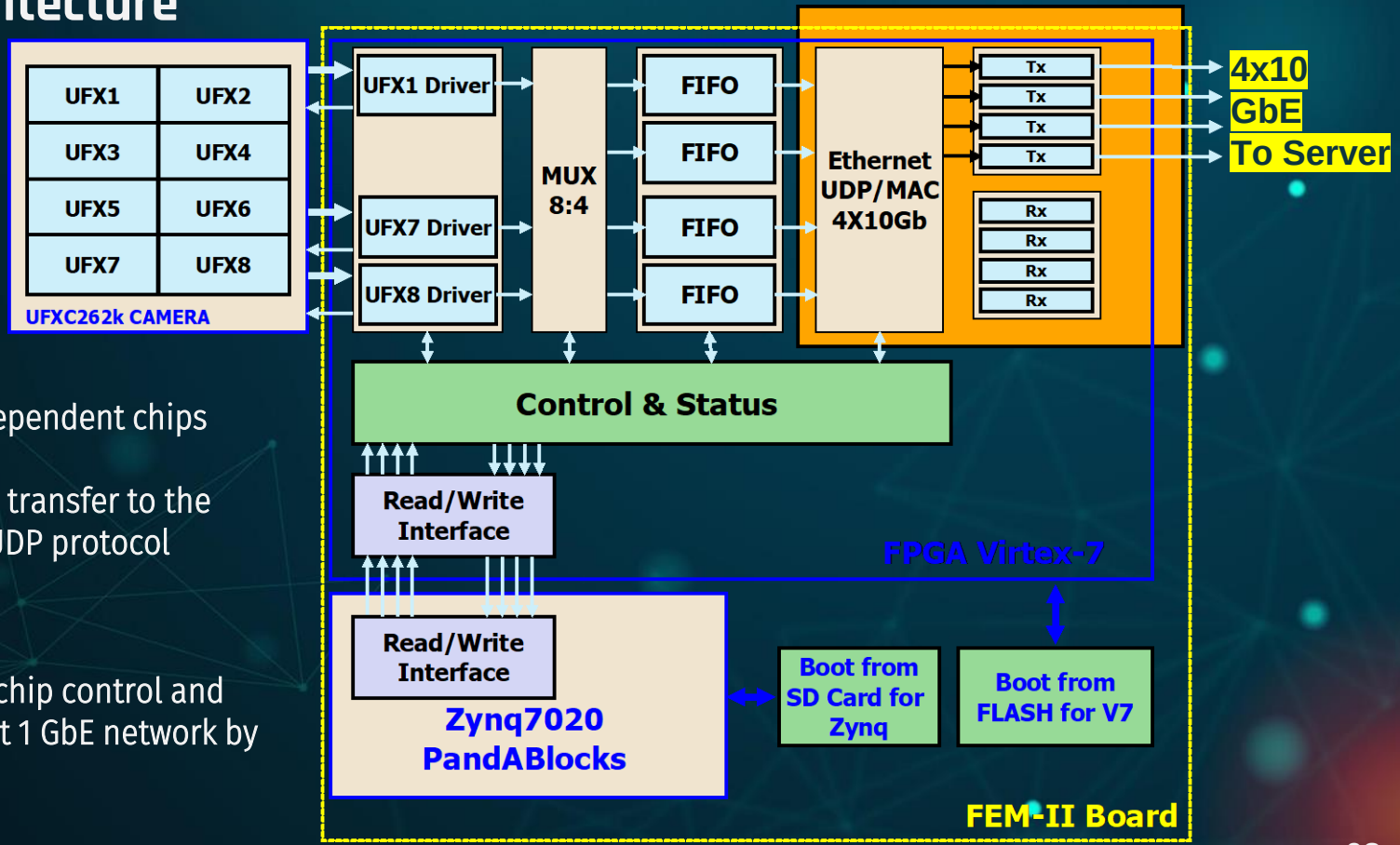
DAQ ARCHITECTURE

1.1 Global Architecture



1.2 DAQ Architecture



- 8 parallel independent chips acquisition
  4x10 GbE data transfer to the Server using UDP protocol

- Independent chip control and status thought 1 GbE network by User

1.3 Control/Status Interface

Why Panda ?

- SoC Zynq: Solution selected to upgrade the FPGA
- To Reduce development time and cost
- Wide set of configurable logic blocks and event sequencer (Function Generators, Timer/Counter, Pulse Generator, SR Gate blocks, etc.)
- Position Compare Trigger Generation
- Analog and Digital I/O support
- LPC/ FMC connector
- Data Capture and Acquisition
- Fully configurable System and Position Bus concept

PandA HW Platform

- 4-Channel Encoders Inputs/ outputs
- Multi-Channel TLL and LVDS Inputs/ outputs
- FMC LPC (fixed to 1,8V), on board clock tree
- 3 SFP (IPBus, Timing, DCC or Custom)
- 1 Gigabit Ethernet for Control and DAQ

PandA Platform Collaboration

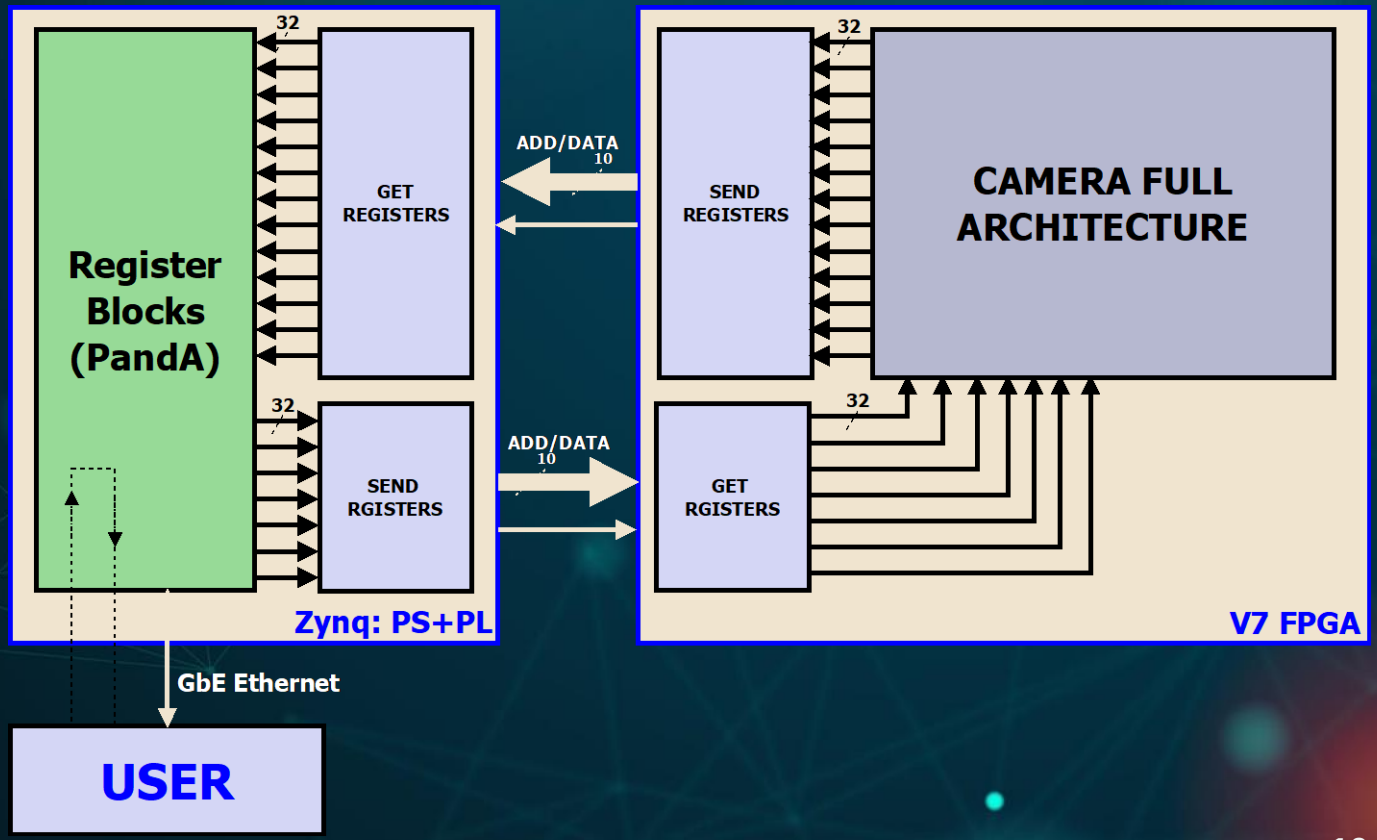
diamond DIAMOND	SOLEIL SYNCHROTRON SOLEIL
FPGA – Zynq Logic Design FPGA – Zynq Processor Design Linux Kernel Development Linux Application Development	Hardware PCB Layout Hardware Schematic Design Mechanical design

Panda not supports 10 GbE + FPGA PL (Zynq) HW resources limitations

1.3 Control/Status Interface

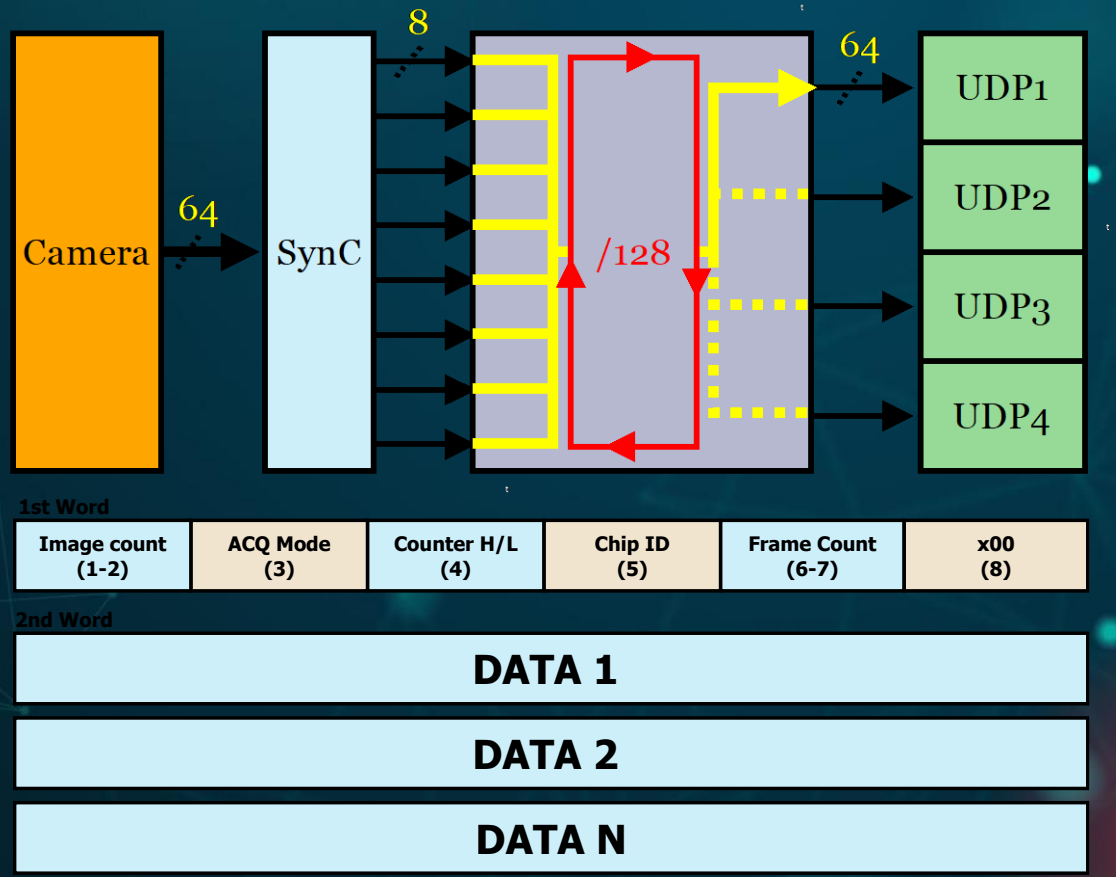
128+128 status/control 32-bits registers fully configurable by user using detector dedicated software API

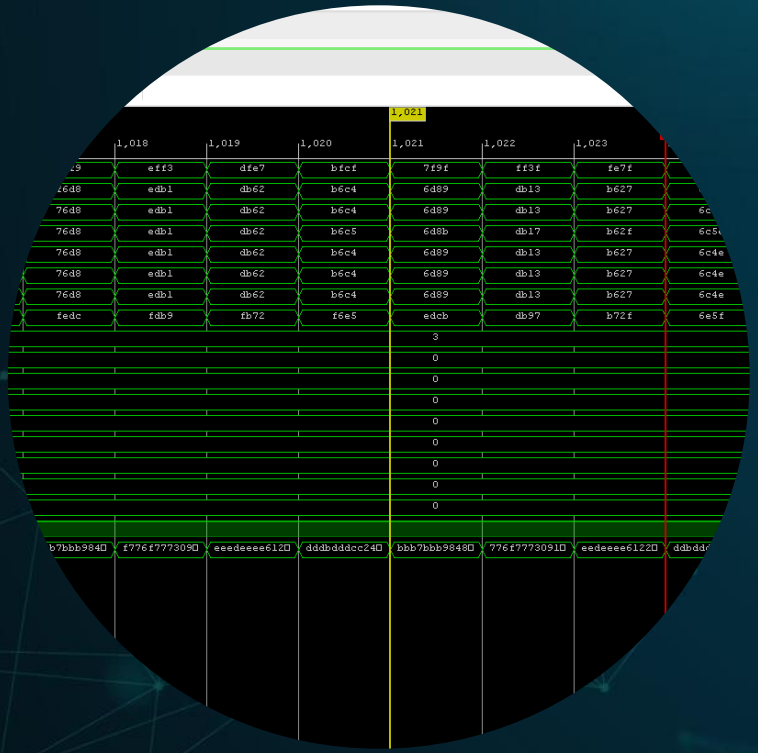
Independent read/write interface between Virtex-7 FPGA and Zynq SoC



1.4 Data packet & Transfert

- Quad-channel UDP 10GbE, 64-bits,156.25 MHz
- 128 words/frame (1024+8 bytes)
- Specific protocol designed to descramble raw image data





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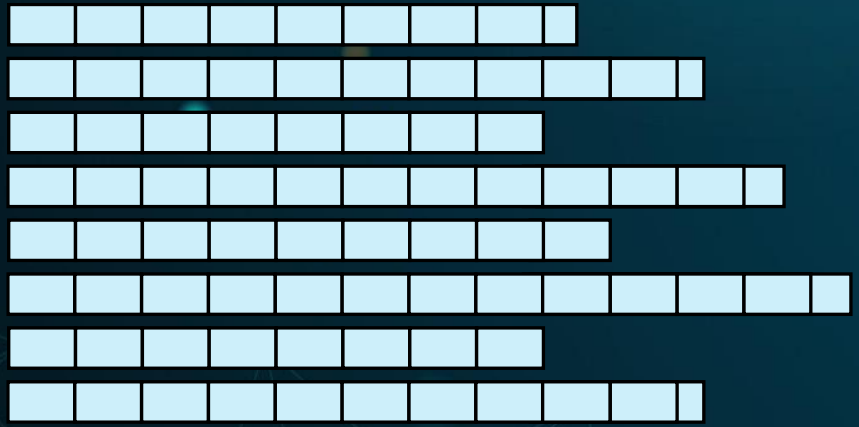
SYNCHRONIZATION PROTOCOLE

3.1 Synchronization Problem



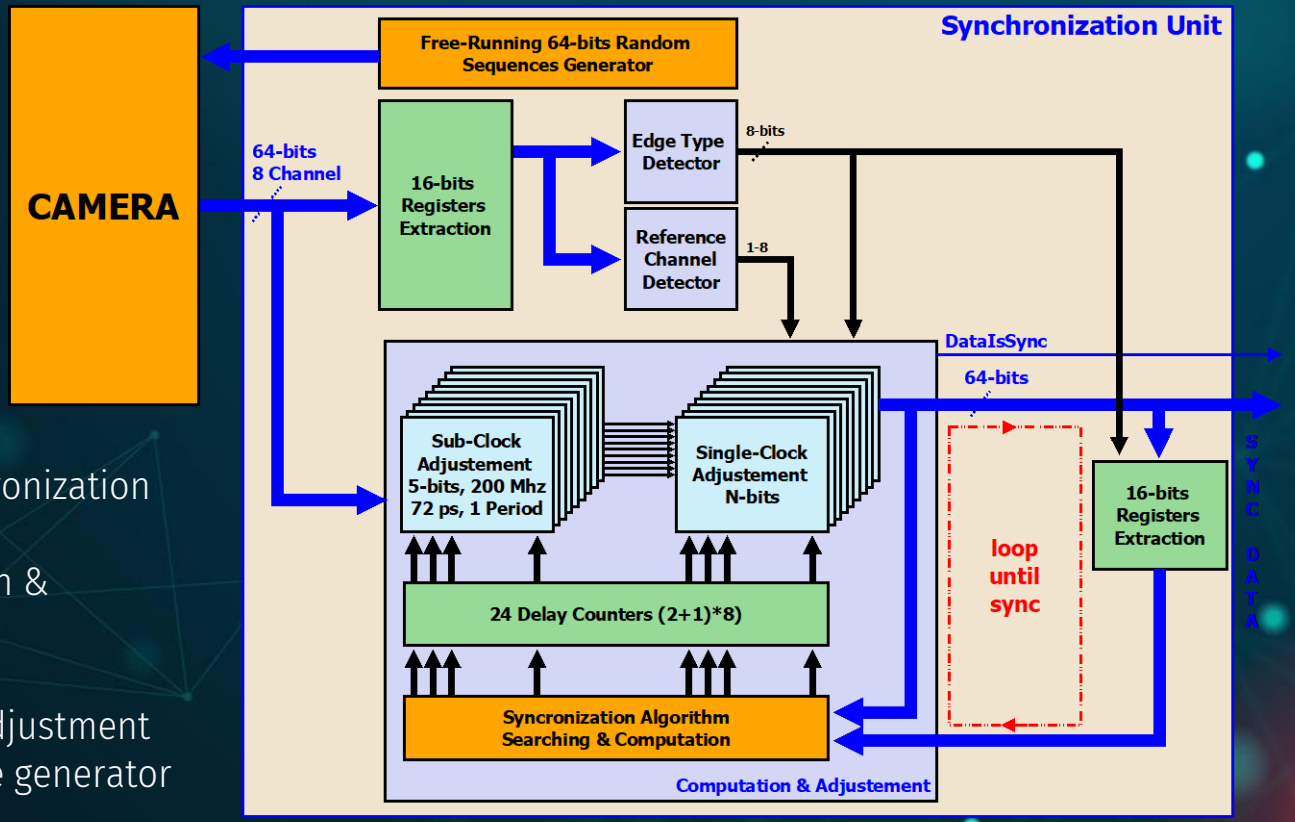
Data Before synchronization

SYNCHRONIZATION

8 Chips data synchronization
8-bits per chips
Asynchronized data ➔ False image descrambling and recovering

Data After synchronization

3.2 Synchronization Architecture

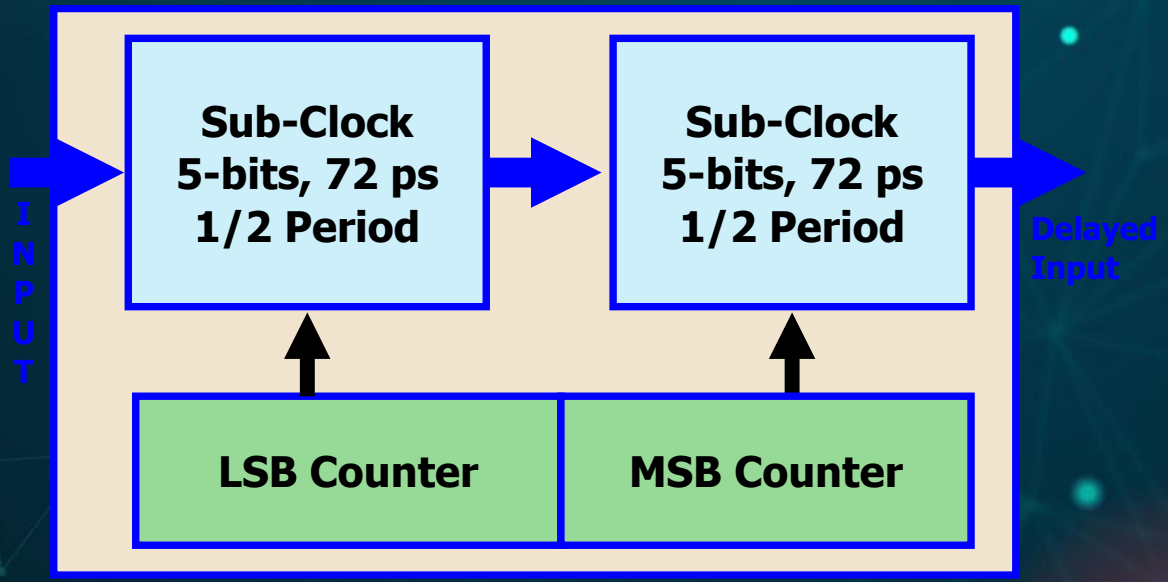


- 8 Channel of 8-bits synchronization
- Sync at camera start-up
- Parallel delay computation & adjustment algorithm
- 72 picosecond resolution
- Sub-cycle & single time adjustment
- 128-bits random sequence generator
- Algorithm convergence

3.3 Delay adjustement bloc

LSB Counter
72 ps resolution, 5-bits
Initialisation each 32 cycles
Incrementation each (128+ random number) clock cycles

MSB Counter
5 ns resolution (1 Clock cycle)
Incrementation when LSB Counter overflow



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CONCLUSION AND PERSPECTIVES

CONCLUSIONS & PERSPECTIVES

Full hardware camera and cooling system were tested with success

1. HARDWARE

Sub-ns Synchronization algorithm has been implemented and tested with success using Virtex-7 FPGA

2. SYNCHRONIZATION

Camera control/status with Zynq has been implemented and tested

Camera data acquisition drivers was done

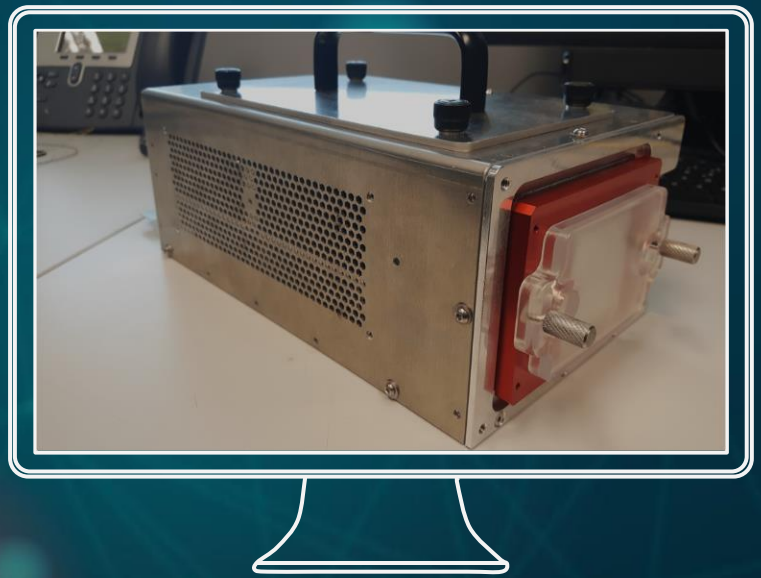
Transfer through UDP ports is on-going: Frame length adjustment is under verification

3. DAQ System

software for image reconstruction is in progress

4. IMAGE RECOVERING

THANKS!



Do you have any questions ?