Integration and Commissioning of the ATLAS Tile Demonstrator Module for Run-3

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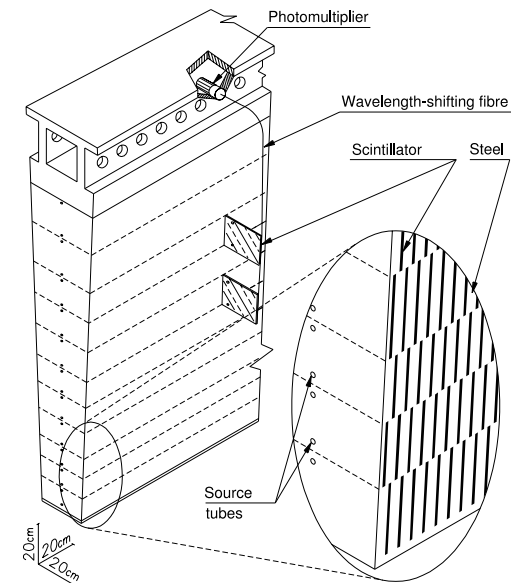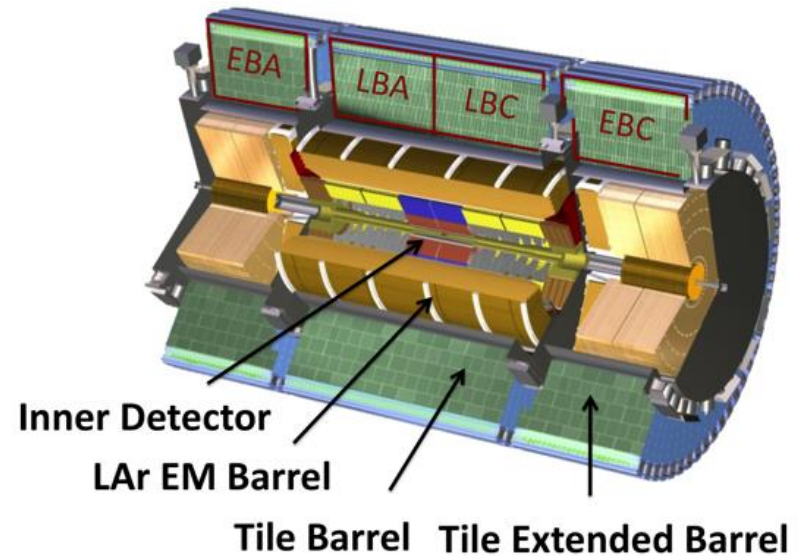on behalf of the ATLAS Tile Calorimeter System

August 5th 2022

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ATLAS Tile Calorimeter

- Central hadronic calorimeter of the ATLAS experiment
  - Covering the central region |η|<1.7

- Contributes to the measurement of energies of hadrons, jets, τ-leptons and E_T^{miss}

- Sampling calorimeter made of steel plates and plastic scintillator tiles
  - Wavelength shifting fibers and 2 PhotoMultiplier Tubes (PMTs) per cell
  - Granularity of $\Delta\eta \times \Delta\varphi = 0.1 \times 0.1$ in most cells
  - Dynamic range from ~10 MeV to ~2 TeV per calorimeter cell

- Divided in 4 partitions: EBA, LBA, LBC, EBC
  - Each partition has 64 wedges modules
    - One module hosts up to 45 PMTs
    - Electronics is located in extractable "*drawers*" at the outermost part of the module
  - 9852 PMT channels for the complete readout

Inner Detector
LAr EM Barrel
Tile Barrel **Tile Extended Barrel**

Photomultiplier
Wavelength-shifting fibre
Scintillator   Steel
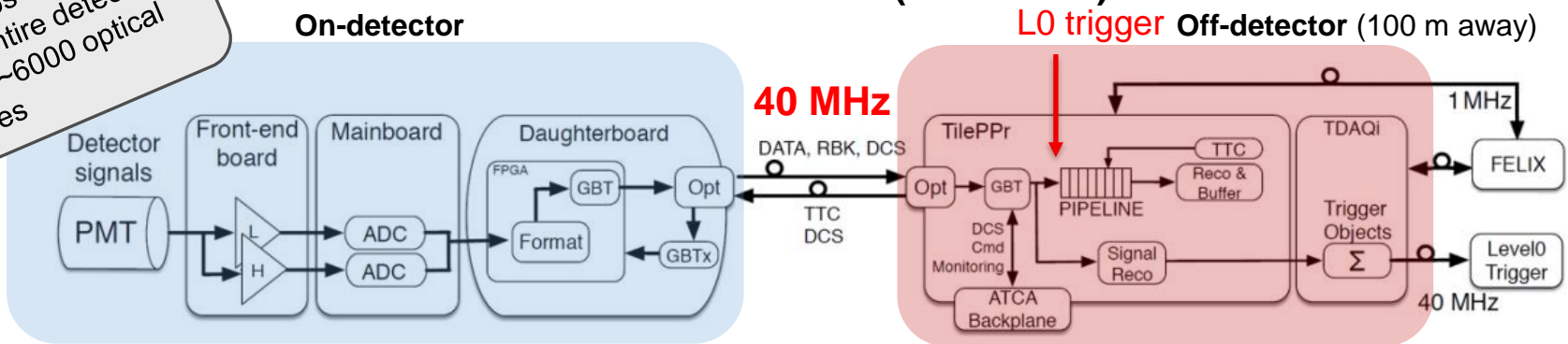Source tubes

TileCal readout architecture at the HL-LHC

- High Luminosity LHC will achieve instantaneous luminosities a factor 5-7 larger than the LHC nominal value around 2029

Current architecture (2011-2025)
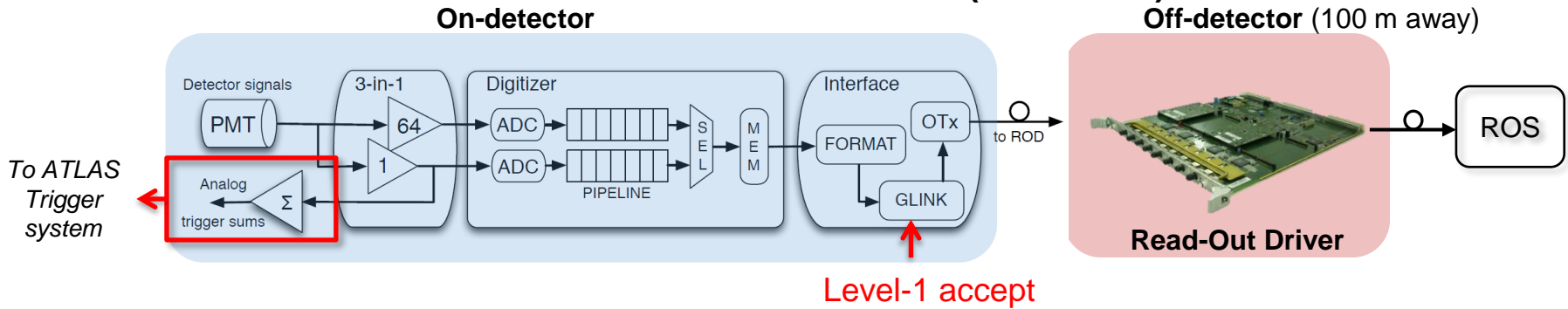
HL-LHC architecture (2029-2040)

Demonstrator Module

- Hybrid module composed of 4 mini-drawers
  - Using the clock and readout strategy for the HL-LHC
  - But providing analog trigger towers information to the ATLAS trigger system

- Each mini-drawer has 2 independent sections for redundant cell read out
  - 12×PMTs & 12×Front-End Boards (FEBs) → read out 6 TileCal cells
  - 1×MainBoard, 1×DaughterBoard, 1×HV distribution board
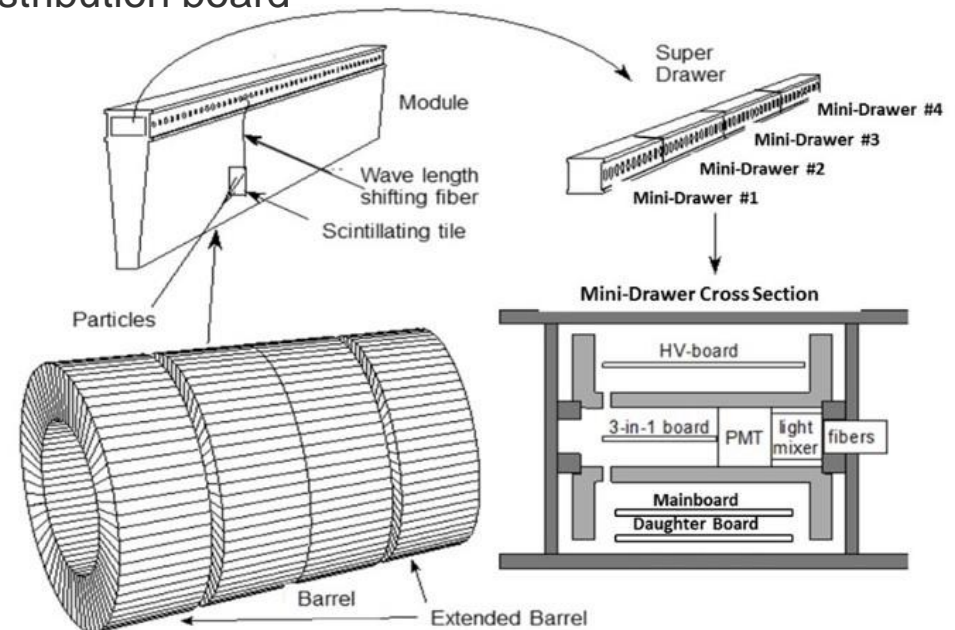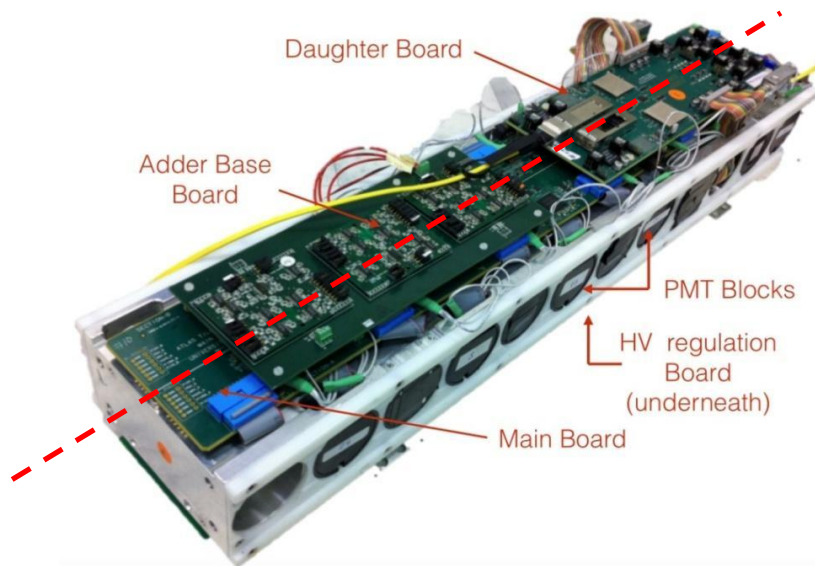
On-detector electronics: FEBs and Active Dividers
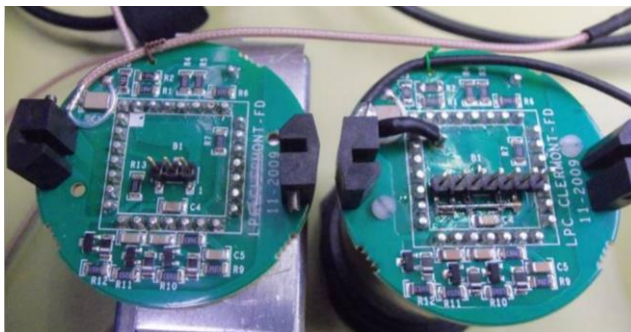

Control & integrator signals

Analog signals

- Front-End Boards: Upgraded 3-in-1 cards
  - Provides PMT pulse shaping with 2 gain amplifications (1:32 ratio -> Low and High gain)
    - Second copy of Low gain signal for analog trigger signals
  - Built-in Charge Injection System for electronics calibration
  - High-precision integrator readout for luminosity measurements and Cs calibration

- Active Dividers
  - Distribute the HV for PMT dynodes using transistors
  - Expected a maximum PMT anode current of 40 µA
  - Provide an excellent linearity up to 100 µA
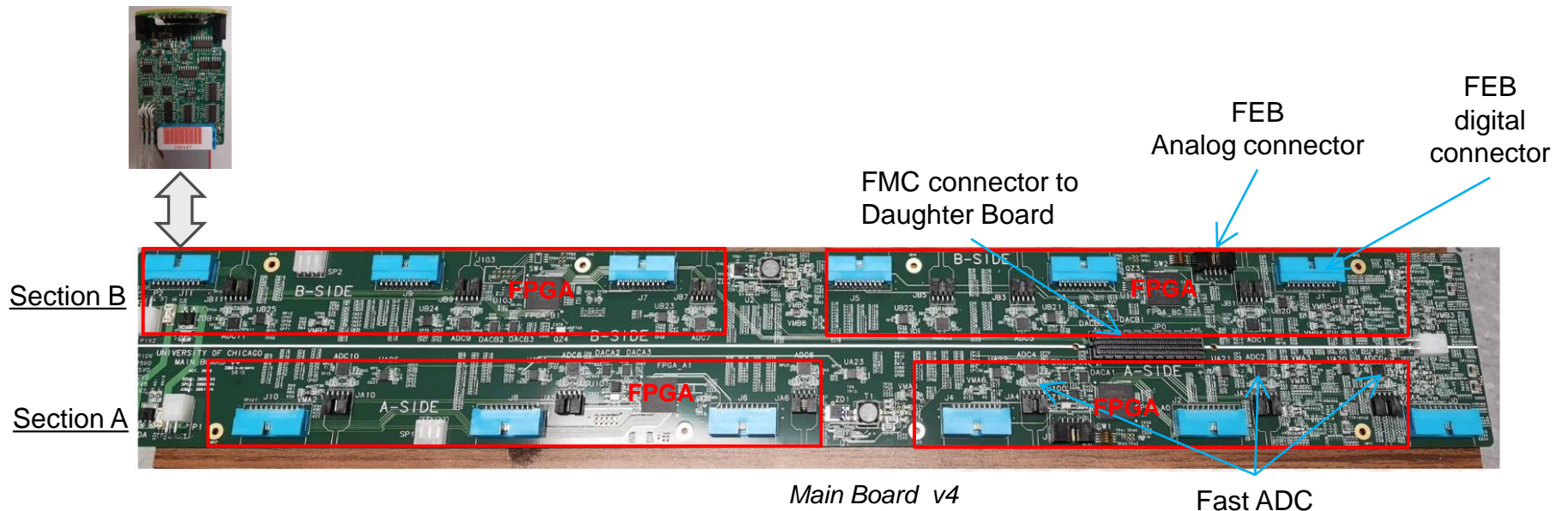
Upgraded 3- in-1 card

Active dividers

On-detector electronics: MainBoard
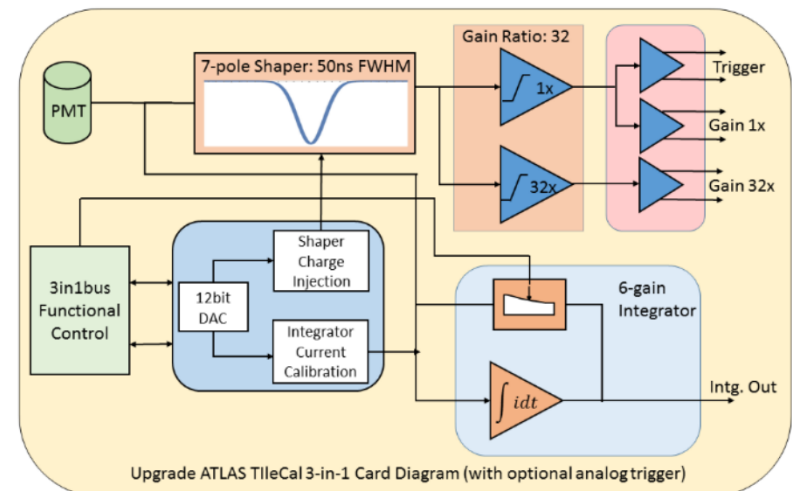
- MainBoard:
  - Digitizes signals coming from 12 FEBs
    - Fast readout: 12-bit dual ADCs @ 40 MSps for 2 gain signals
    - Slow readout : 16-bit SAR ADCs @ 50kSps for integrator readout
  - Provides digital control and configuration of FEBs + high-speed path to the DaughterBoard
  - Divided in two halves for redundancy → readout and power distribution

Section B

Section A

FMC connector to Daughter Board

FEB Analog connector

FEB digital connector

Fast ADC

Main Board v4

On-detector electronics: DaughterBoard

- High-speed interface with the off-detector electronics
  - Collection of PMT digitized data from Mainboards and transmission to off-detector electronics
  - Clock and command distribution to FEBs
  - Data link redundancy
- DaughterBoard v4 installed in Demonstrator
  - 2 × GBTx chips for LHC clock recovery and distribution
  - 2 × Kintex 7 FPGAs for communication and data processing
  - 2 × QSFP optical modules
- Possible upgrade to DaughterBoard v6 this year
  - Kintex UltraScale FPGAs and improved clock quality

Power distribution system

FPGAs

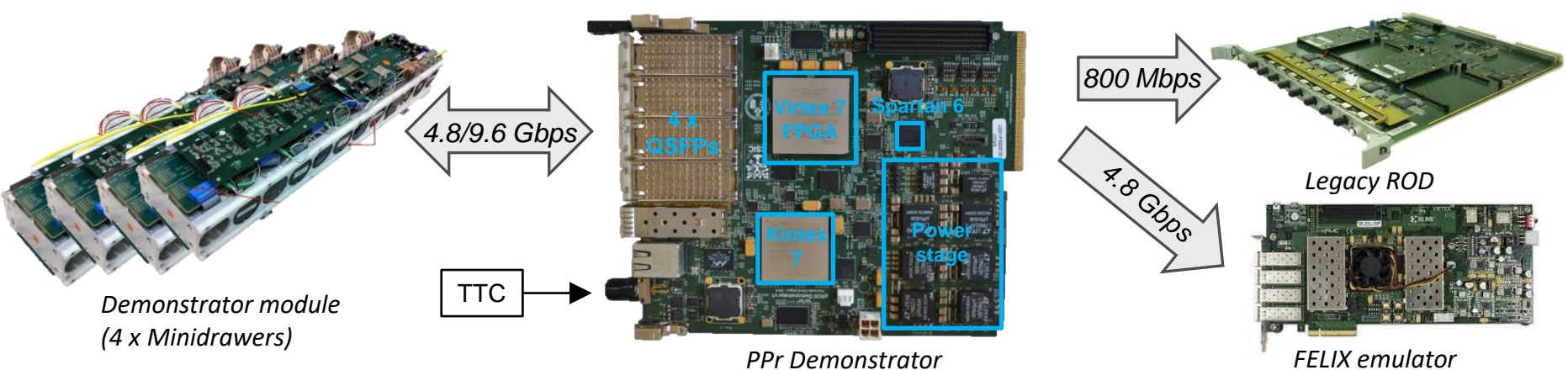GBTx

Section A

Section B

2 x QSFPs
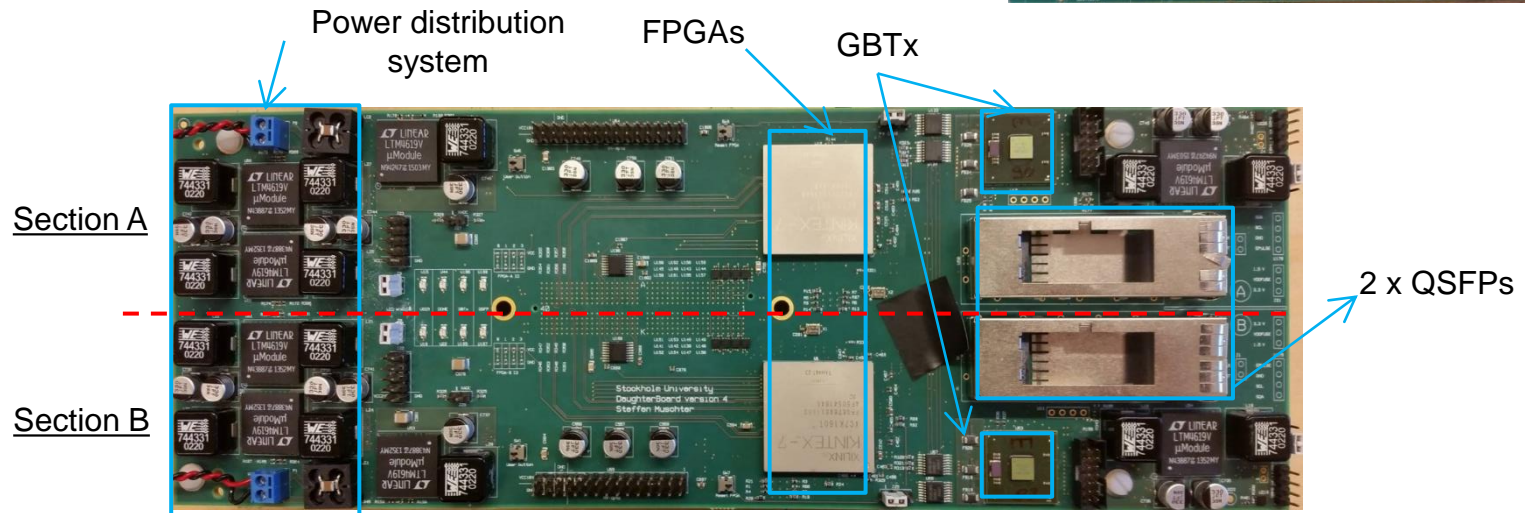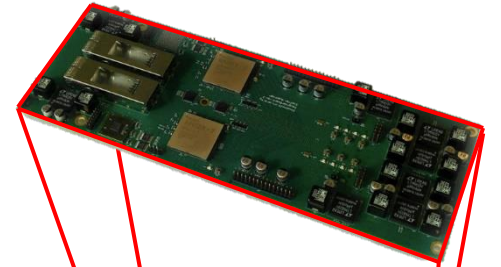
Off-detector electronics: PreProcessor Demonstrator

- Off-detector readout system based on FPGAs and high-speed modules
  - Data acquisition and processing @ 40 MHz
  - Distribution of the LHC clock towards the on-detector electronics
  - Interface with the ATLAS readout system

- Double AMC board equipped with 4 QSFPs, Virtex 7, Kintex 7 and Spartan 6
  - Capable of operating 1 upgraded TileCal module → up to 4 Mini-drawers
  - Operated in an ATCA shelf 100 meters away from the detector

- Enables backward compatibility between the Demonstrator and the current ATLAS TDAQ system
  - Communication with the Timing, Trigger and Control (TTC) system
  - Triggered events are transferred to the ReadOut Drivers and FELIX system

- Possible upgrade to final version → Compact Processing Module

Compact Processing Module

Demonstrator module (4 x Minidrawers)

4.8/9.6 Gbps

TTC

PPr Demonstrator

800 Mbps

4.8 Gbps

Legacy ROD

FELIX emulator

Firmware implementation

- Links configured for fixed and deterministic latency
  - Downlinks: 4 GBT links at 4.8 Gbps → Clock and configuration
  - Uplinks: 4 GBT links at 9.6 Gbps → Data samples, monitoring, sync

  per mini-drawer
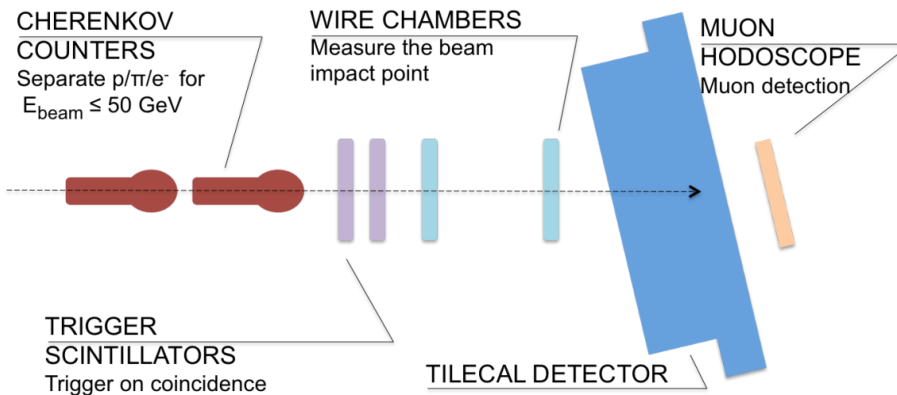

on-detector   *off-detector*
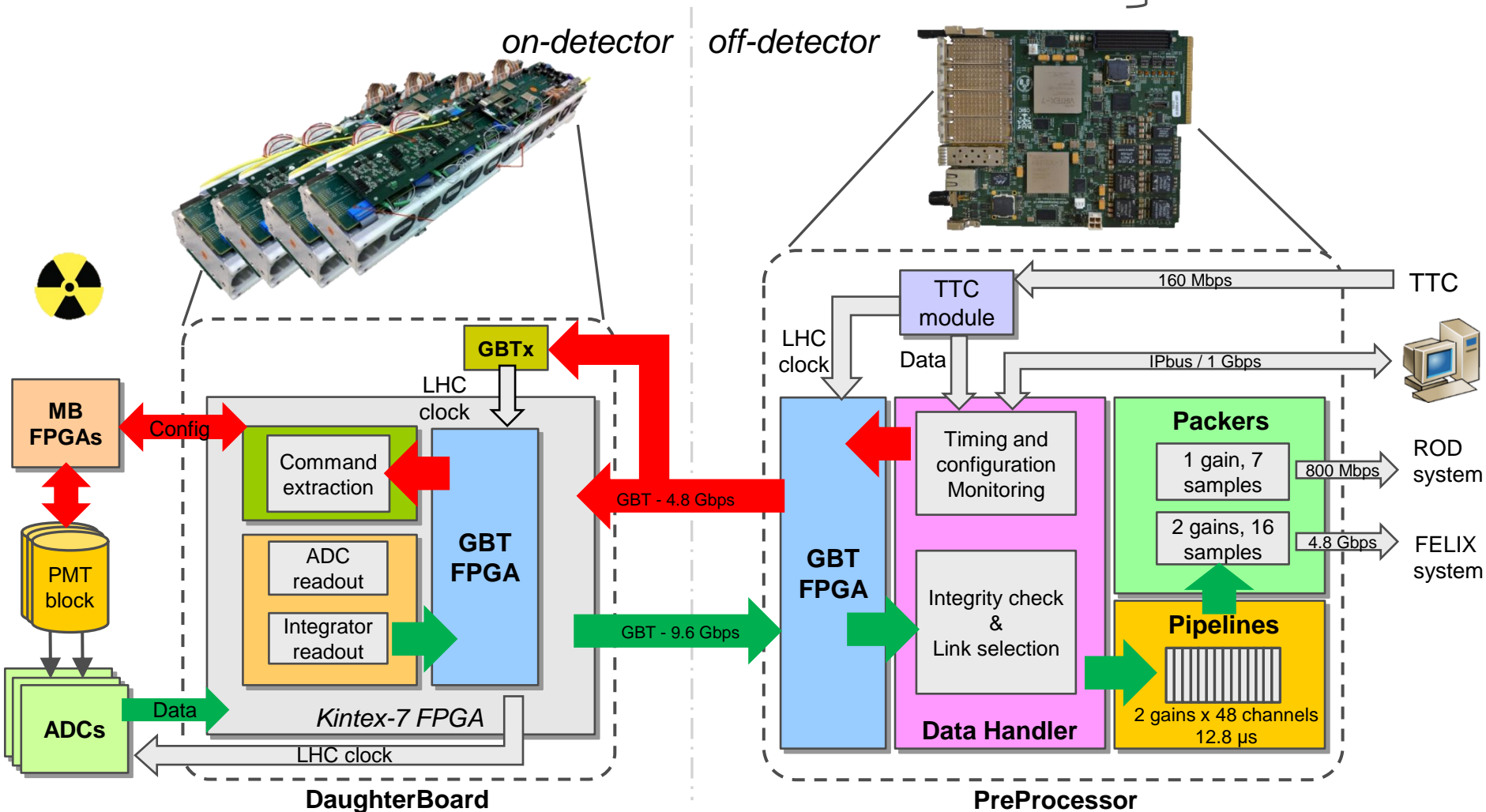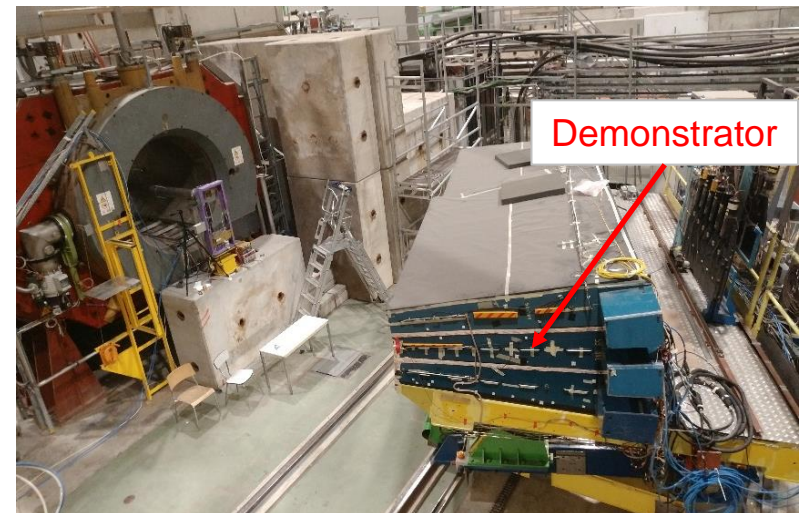
Demonstrator construction and test beams

- Demonstrator module was initially built in 2015
  - Latest versions of the upgraded readout electronics & mechanics

- Seven test beam campaigns between 2015 and 2018 at the North Area of the SPS accelerator (CERN)
  - Detector modules equipped with upgraded and legacy electronics for performance comparison

- Beams of hadrons, electrons and muons at different energy ranges and projective angles
  - Study the calorimeter response and S/N performance of the new electronics

First Demonstrator

CHERENKOV COUNTERS
Separate $p/\pi/e^-$ for $E_{beam} \le 50$ GeV

WIRE CHAMBERS
Measure the beam impact point

MUON HODOSCOPE
Muon detection

TRIGGER SCINTILLATORS
Trigger on coincidence

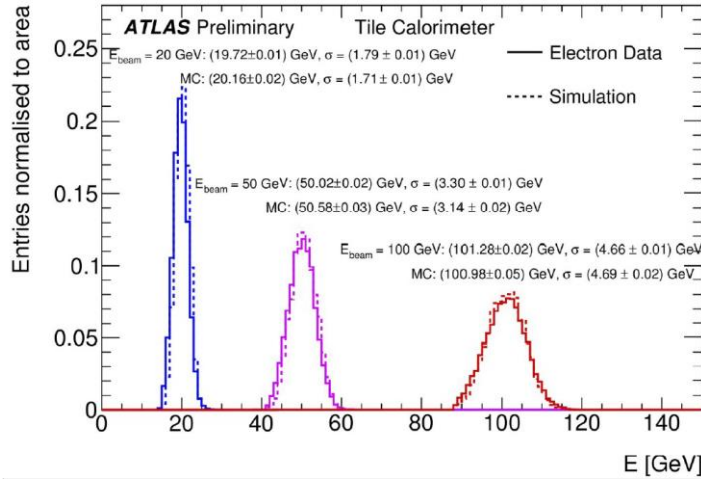TILECAL DETECTOR

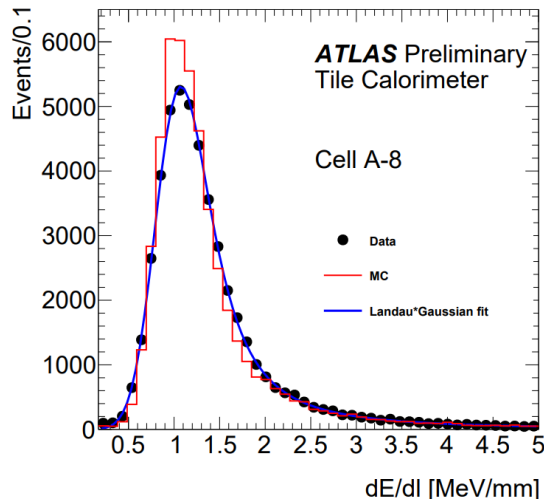*Beam line elements*

Demonstrator

Test beam setup at SPS
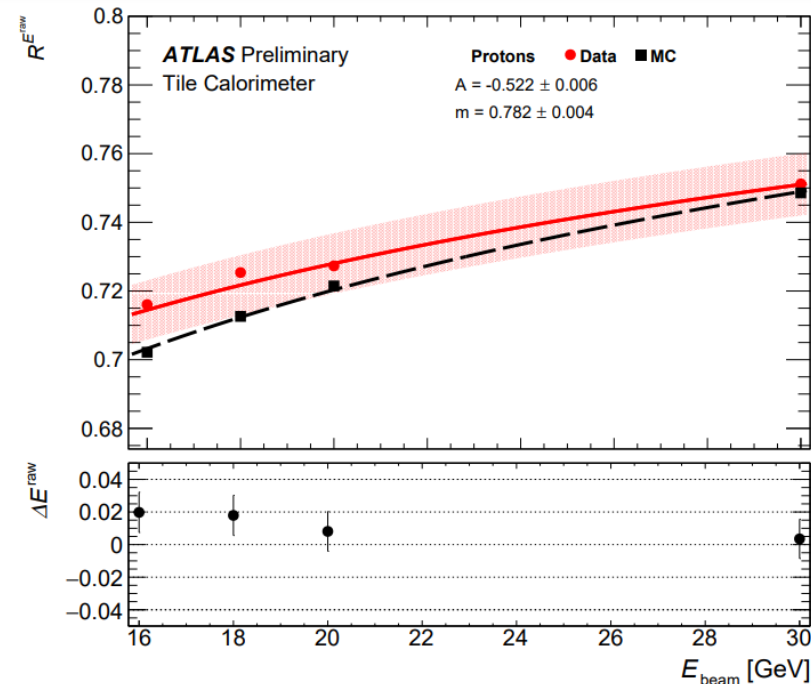
Test beam results

- Data to Monte Carlo response with hadrons, electrons and muons

Calibration for detector response to beams of single electrons better than 2%

Energy losses of muons per length of the path in the cell A8 (cell in the inner most layer) measured at -90˚


Energy response ratios, $R^{\langle E^{raw}\rangle} = \dfrac{E^{raw}}{E^{raw}_{beam}}$, as function of the proton beam energy. Ranges of measured/MC variations are within 2.5%

Insertion in the ATLAS experiment

- Demonstrator module inserted in ATLAS July 2019
  - Exercised during the LHC Long Shutdown 2 (2019-2021)

- Operating with backward compatibility with the current ATLAS DAQ system
  - Clock and configuration commands from legacy TTC
  - Triggered event data transmitted to ATLAS DAQ
  - Provides analog cell sums to the ATLAS trigger system


Insertion of the Demonstrator in LBA
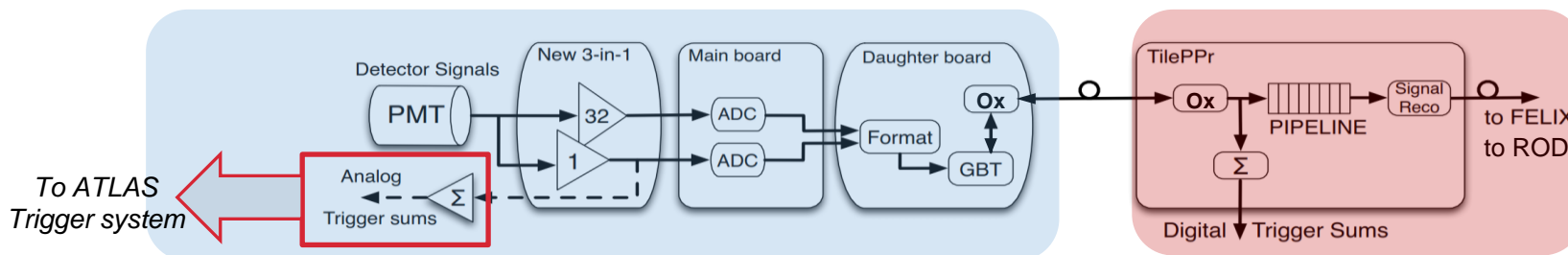
- Fully integrated with the TDAQ and Detector Control System (DCS) softwares
  - Front-end electronics configuration
  - Physics, calibration and laser runs
  - Event builder, offline reconstruction, data quality monitoring
  - HV and LV control and monitoring through the DCS software

Comissioning and operation
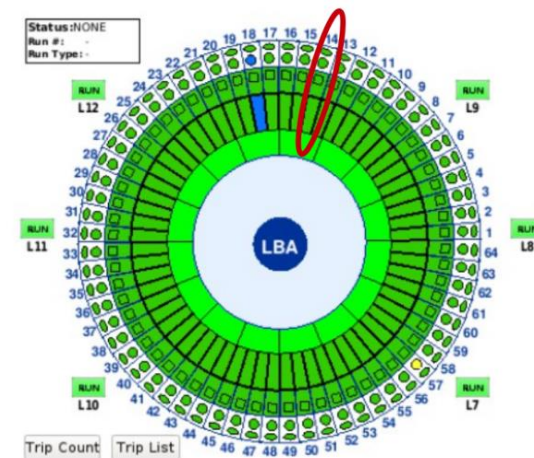
- Evaluation of the signal quality between the Demonstrator and the PreProcessor using embedded FPGA resources
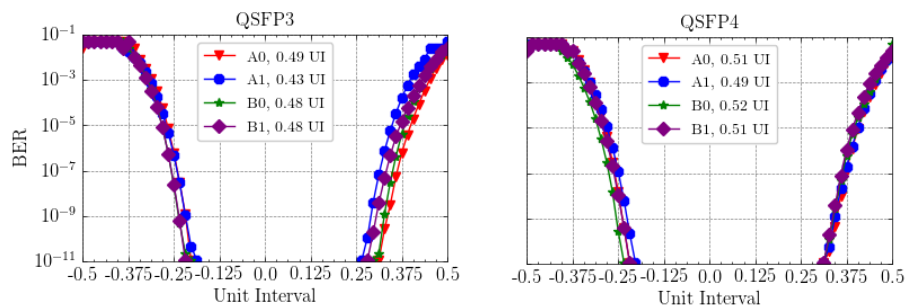
BER test for the Demonstrator uplinks
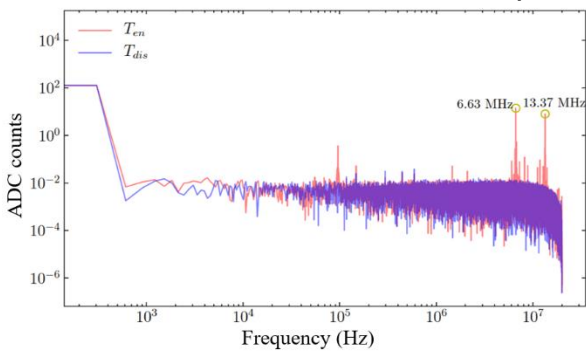
FFT analysis of the pedestal data of a noisy trigger output

Event display of a collision event at 13.6 TeV recorded in ATLAS on 5th July 2022

- Comissioning of the analog trigger towers
  - Detection of noisy trigger outputs during installation

- Recorded multiple runs with cosmics rays, LHC splash events, laser and CIS
  - Recorded first events at 13.6 TeV this July!

- Demonstrator shows a good and stable performance

Summary

- New conditions imposed by HL-LHC requires a redesign of the TileCal on-detector and off-detector electronics with a new clock and data readout strategy

- Construction of a "hybrid" upgraded module and off-detector prototypes
  - Extensively exercised during seven test beam campaigns (2015-2018)

- Demonstrator module inserted and commissioned in ATLAS between 2019-2022
  - Implements the clock and readout architecture for the HL-LHC
  - Backward compatibility with the current ATLAS TDAQ and DCS systems
 - Ready for taking data in the ATLAS experiment for Run-3 (2022-2025)!
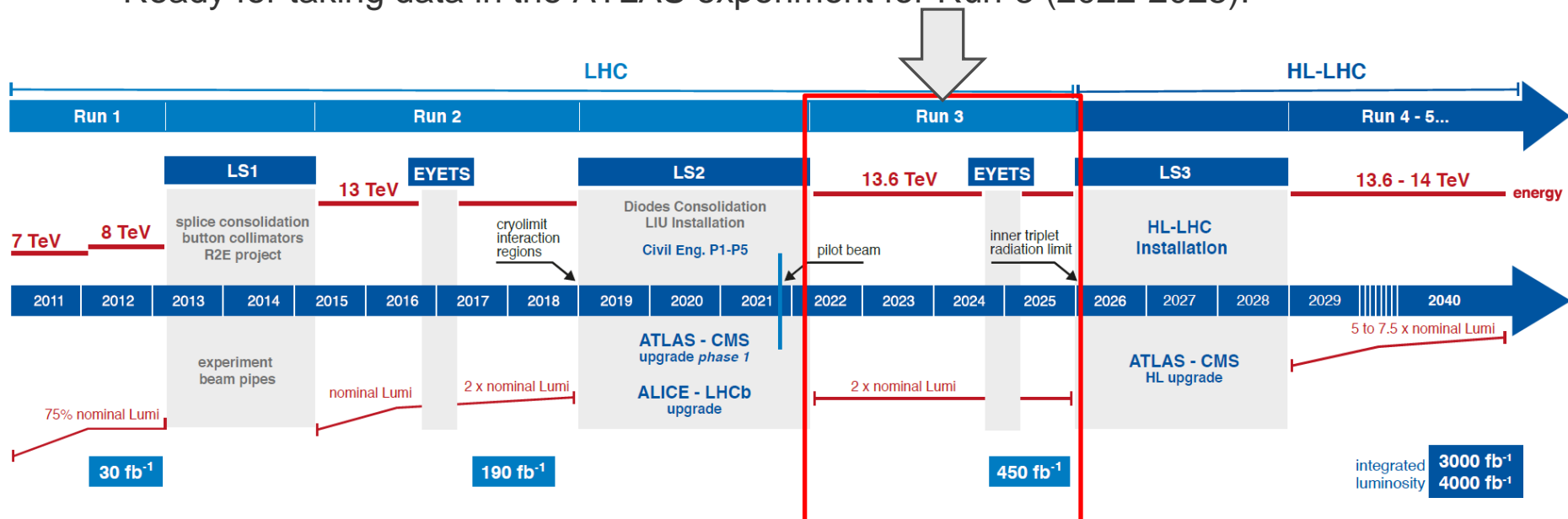
THANKS FOR YOUR ATTENTION

Low and High Voltage system

- Three stage system with redundancy
  - 200V from off-detector
  - 8 redundant bricks per mini-drawer (LVPS) to power 4 mini-drawers with 10V
  - Point-of-Load regulators at the Mainboards and DaughterBoards

- Fully control and monitoring from the ATLAS DCS system

Bricks
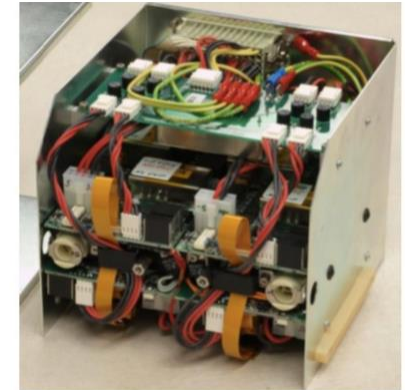
Low Voltage Power Supply

HV distribution board

48-channels HV remote board

- HV remote boards located off-detector → up to 48 PMTs
  - Provide individual control, monitoring and regulation per PMT
  - Easy access and avoid radiation issues
- HV distribution board per mini-drawer in the on-detector → up to 12 PMTs
- 100 meter long HV cables → 48 pairs of wires

GigaBit Transceiver Protocol

- Data protocol between the DaughterBoards and the TilePPr

- Developed by CERN for data communcation in radiation enviroments
  - GBTx, LpGBT, GBT-SCA chips

- Main features

Frame	Wide-Bus
3.2 Gbps	4.48 Gbps

  - 120 bit words @40 MHz → **4.8 Gbps**
  - Forward Error Correction capabilities
    - Reed Solomon encoding → up to 16 consecutive error bits

- Two possible implementations in FPGA:

- **Standard:** easy implementation, but no fixed and determinitisc latency

- **Latency Optimized (LO):** fixed and deterministic latency at the cost of a complex implementation

119   0

4 bits	4 bits	80 bits	32 bits
Header	Slow Control	Data	FEC

Tile GBT implementation

- Implementation of 16 LO GBT links in the TilePPr
  - Downlink: GBT code with minor modifications

    not enough bandwidth → **5.76 Gbps only for the PMT samples!**
  - Uplink: not enough clock resources

    time stamp the data → RX and TX clocks are not in phase

- Two important modifications on the original GBT code
  - Data rate increased by factor two: from 4.8 Gbps to 9.6 Gbps
  - BO-CDR → optimization of clocking resources and data retiming