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# Application of the IEC61508 standard to carry out the Verification and Validation process of FPGA-based Intelligent Acquisition Systems designed using OpenCL-HLS

The use of Field Programmable Gate Array (FPGA) based systems are becoming more widespread within Intelligent Instrumentation and Control (I&C) field. This is due to the advantages they offer in terms of timing, versatility and safeness against cyber-attacks. Traditionally, these devices had been mostly programmed using low-level Hardware Description Languages (HDL), but the use of high-level HDL based on C/C++, such as OpenCL or HLS, or graphical programming languages is increasing considerably. Moreover, many of these FPGA-based I&C applications are involved in Investment Protection Systems, which demand high-reliability and safety solutions. Ensuring reliability to an acceptable level requires a hard and high timing consuming Verification and Validation (V&V) process compliant with some applicable standards. Currently, there is no specific safety standard fully oriented to systems designed using high-level Hardware Description Languages, so conventional methodologies and standards must be adapted.

This paper proposes a V&V methodology according to the requirements of the IEC 61508 standard applicable to systems designed using High-Level HDL. In particular, this work presents results of an in-depth study of the limitations and possibilities of this V&V methodology for different technologies and design cycles, as well as devices from different manufacturers are used. A unified methodology is proposed, that incorporates the use of current verification strategies, based on System Verilog and Universal Verification Methodology (UVM), together with a set of verification tools to check quality of the code or perform simulations from third-party vendors.

## Minioral

Yes

## IEEE Member

No

## Are you a student?

No

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