Verification and Validation of ITER Interlock System Fast Architecture according to IEC 61508 standard

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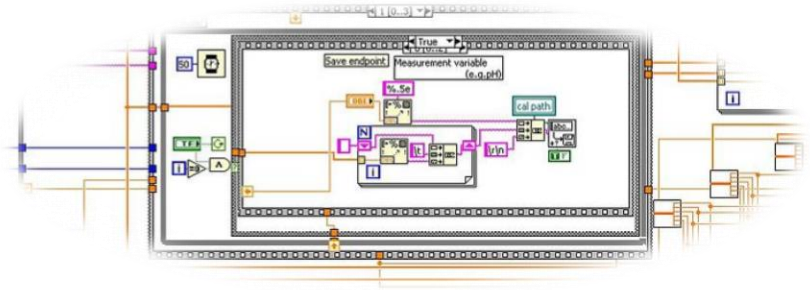
- Interlock Fast Architecture based on National Instruments CompactRIO hardware.

- "Double-decker" solution. Two NI9159 chassis running in parallel.

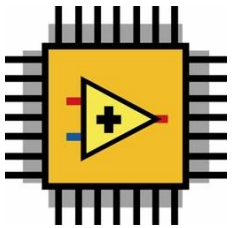
- LabVIEW FPGA as developing tool.



LabVIEW Graphic Code (User)

```
5  entity signed_adder is
6    port
7    (
8      aclr : in   std_logic;
9      clk  : in   std_logic;
10     a    : in   std_logic_vector;
11     b    : in   std_logic_vector;
12     q    : out  std_logic_vector
13   );
14 end signed_adder;
15
16 architecture signed_adder_arch of signed_adder is
17   signal q_s : signed(a'high+1 downto 0); -- extra bit wide
18
19 begin -- architecture
20   assert(a'length >= b'length)
21     report "Port A must be the longer vector if different sizes!"
```

Autogenerated VHDL Code (NI and Xilinx tools)



NI FPGA programmed

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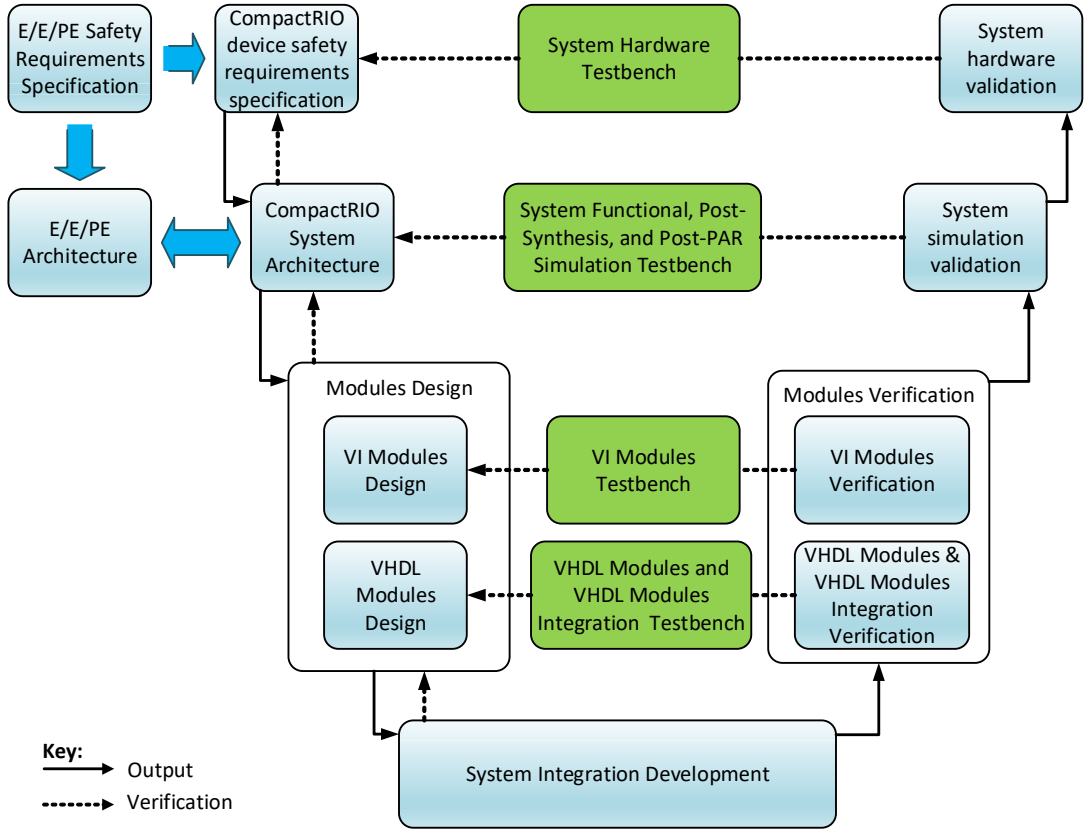
- IEC 61508 is developed for HDL, not for high-level synthesis languages or graphical languages.
- ITER has the challenge to develop the FA with failure-per-hour similar to IEC61508 SIL-3 (3IL-3).
- Verification and Validation process was carried out on a previous developed plant system.
- Extracting the possibilities and limitations.



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