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Analysis of the portability of a testing exchangeability using a randomized power martingale algorithm in FPGA-based devices

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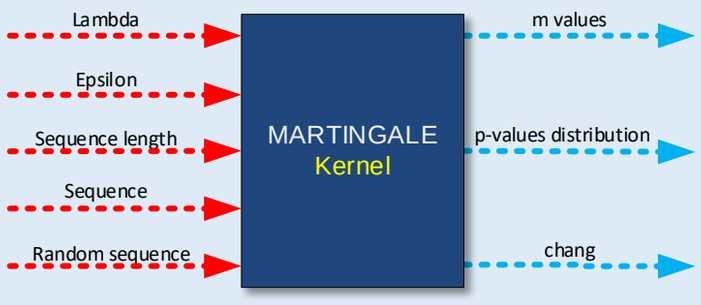
Abstract

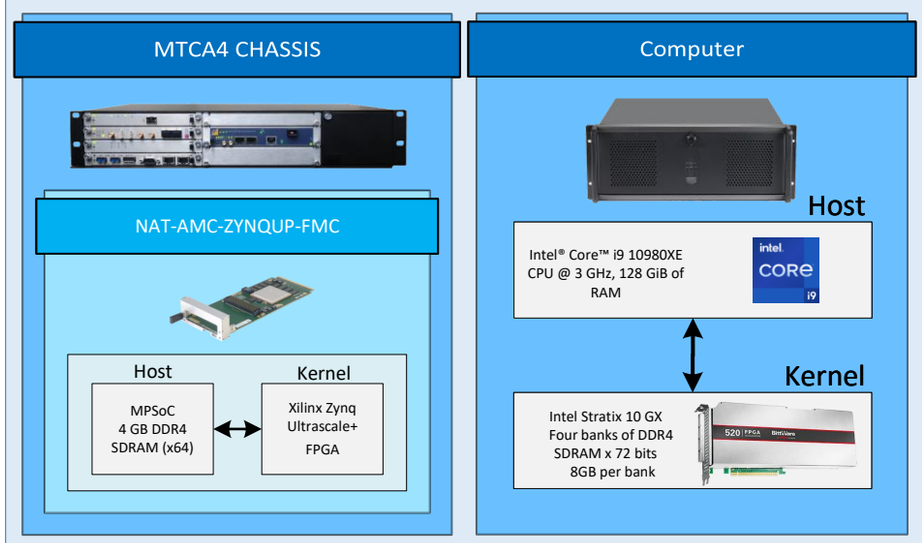
Event detection in fusion experiments is essential for plasma control during discharges and requires fast data acquisition and processing to meet real-time constraints, which demands the implementation of FPGA-based data acquisition and detection systems. The randomized power martingale RPM algorithm deals with the changing nature of a multidimensional dataset, detecting changes in the data distribution. This work presents the implementation using the OpenCL language of such an algorithm in two FPGA-based devices and the performance obtained. The development and tests have been done in a Micro Telecommunications Computing Architecture (MTCA) platform using two Advanced Mezzanine Cards boards, including an ARRIA10 device from INTEL FPGA and a ZynqMP from XILINX respectively. The contribution details: the development cycle followed to do the implementation, the optimization techniques used and the performance obtained, and the conclusions about the portability of the solution achieved. It is worthy that some details about the comparison between OpenCl and HLS are also provided.

1 - Algorithm

- The martingale algorithm has been applied in the fusion field to detect variations in the 3D spatial distribution of the plasma volume emission intensity.
- The algorithm must decide whether a change in the data distribution has occurred when a new sample arrives. The mathematical foundations can be found in previous works [1] [2].
- Both implementation of this algorithm (Xilinx HLS and OpenCL) share inputs and outputs



2 - Platforms used for the implementation-evaluation

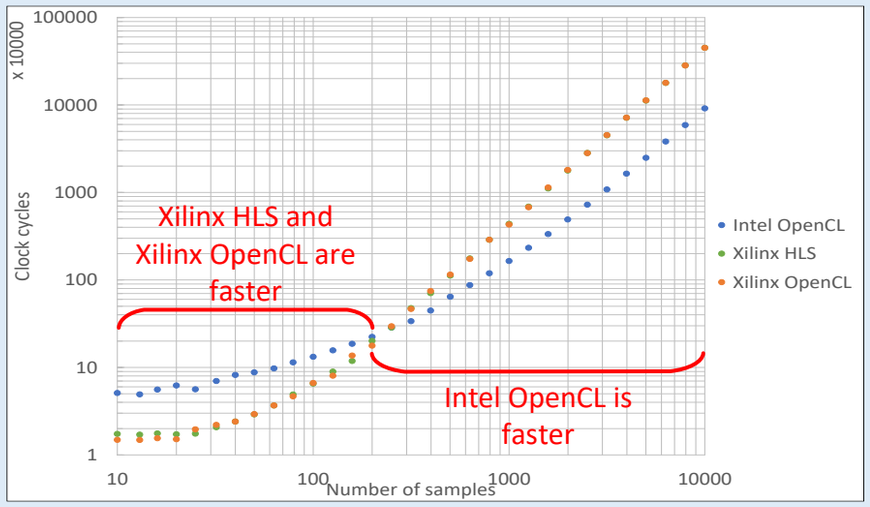


3 - Development

- The martingale algorithm was developed for **OpenCL** initially and adapted to Xilinx HLS afterwards with as few changes as possible to compare them.
- The algorithm has been implemented using floating point to preserve accuracy.
- One of the algorithm input is a set of random values, which is used to detect the violation of data exchangeability. This set is calculated in the host previously to executing the kernel to avoid complexity in the FPGA and to save FPGA resources.
- The host application has been written in C++ using the OpenCL C API, due to being the one supported by both manufacturers, however, Xilinx also offers XRT and the OpenCL C++ wrapper API.
- In Xilinx the kernel needed minimal changes to adapt it from OpenCL to HLS.

4 - Results

- Devices used have been Bitware Stratix 10 (Intel) and NAMC-ZYNQUP-FMC (Xilinx)
- All tests were executed using the same input data.
- Clock cycles were obtained by measuring kernel execution times and dividing by the board frequency.
  - Bitware Stratix 10: 480 MHz
  - NAMC-ZYNQUP-FMC: 200 MHz



5 - Conclusions

- Migrating from platform or from OpenCL to Xilinx HLS has been shown to be simple and straightforward, however, were the kernel use propietary instructions, these would need to be adapted, which in some cases would make the process more difficult.
- Performace differences between Xilinx HLS and Xilinx OpenCL seem to be negligible for the algorithm implemented.
- In a first approach, performance in Xilinx platform is faster for small number of samples, while Intel is faster for bigger numbers.

References

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