Software based readout driver evolution towards 1 MHz readout as part of the ATLAS HL-LHC upgrade

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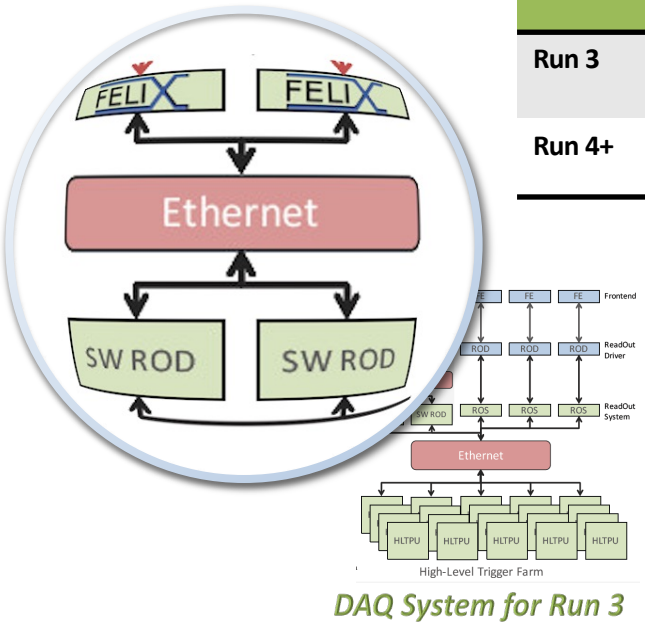
ATLAS Readout System Evolution for HL-LHC

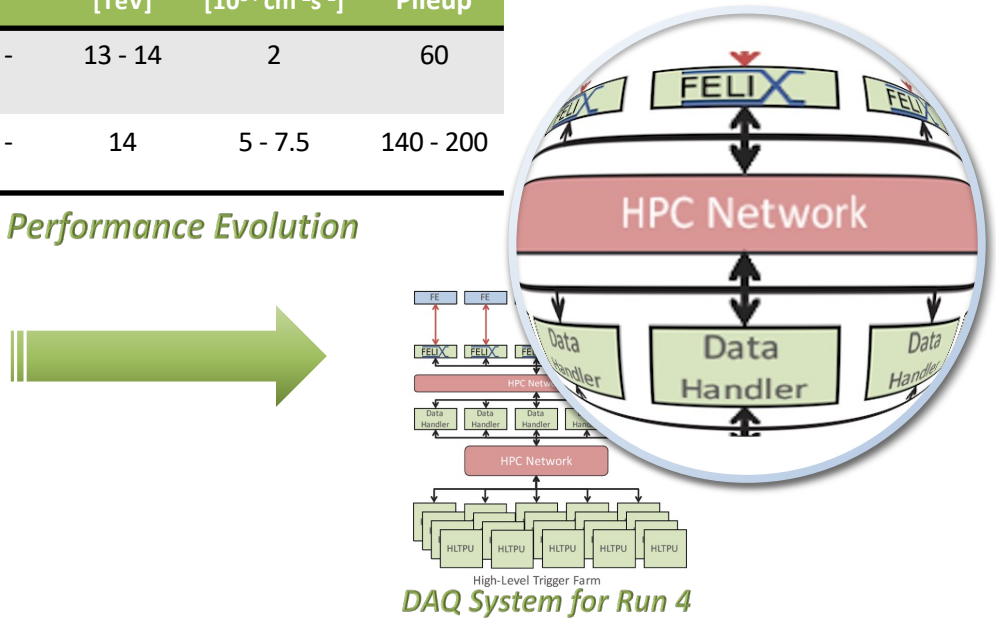
Run 3: SW ROD	Run 4: Data Handler
100 kHz Level 1 Rate	**1 MHz Level 1 Rate**
A fraction of the Readout	Full Readout
The same functional requirements: A SW Component to receive data and perform event building	

	Period	Energy [TeV]	Peak Lumi [10^{34} cm^{-2}s^{-1}]	Peak Pileup
Run 3	2022 - 2024	13 - 14	2	60
Run 4+	2027 -	14	5 - 7.5	140 - 200

LHC Performance Evolution



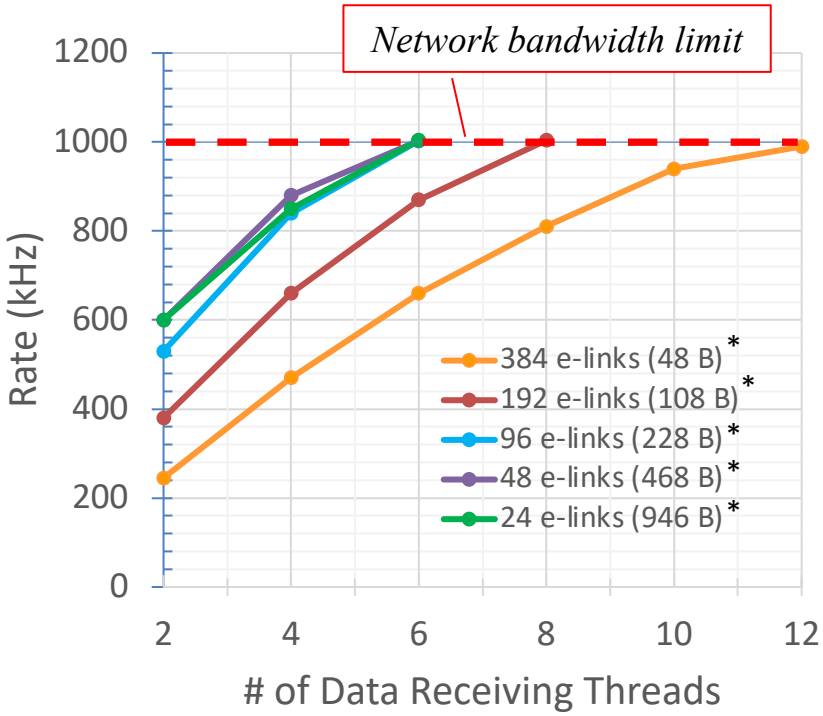
DAQ System for Run 3



DAQ System for Run 4

Run 3 SW ROD Scaling towards Run 4 Requirements

- Can build events at **1 MHz** rate from data packets received from up to **384 input links**
- Using up to 12 CPU cores of the Run 3 SW ROD computer:
  - Dual **Intel(R) Xeon(R) Gold 5218** CPU @ 2.30GHz (16x2 cores)
  - 96 GB of RAM
- Performance scales almost linearly with both:
  - Number of input links
  - Data packets size



**Packet sizes account for the overhead of the currently used custom network protocol built on top of RoCE*