CAEN Electronic Instrumentation

Tools for Discovery

Future perspective of Digital DAQ

Yuri Venturini (y.venturini@caen.it)

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Introduction

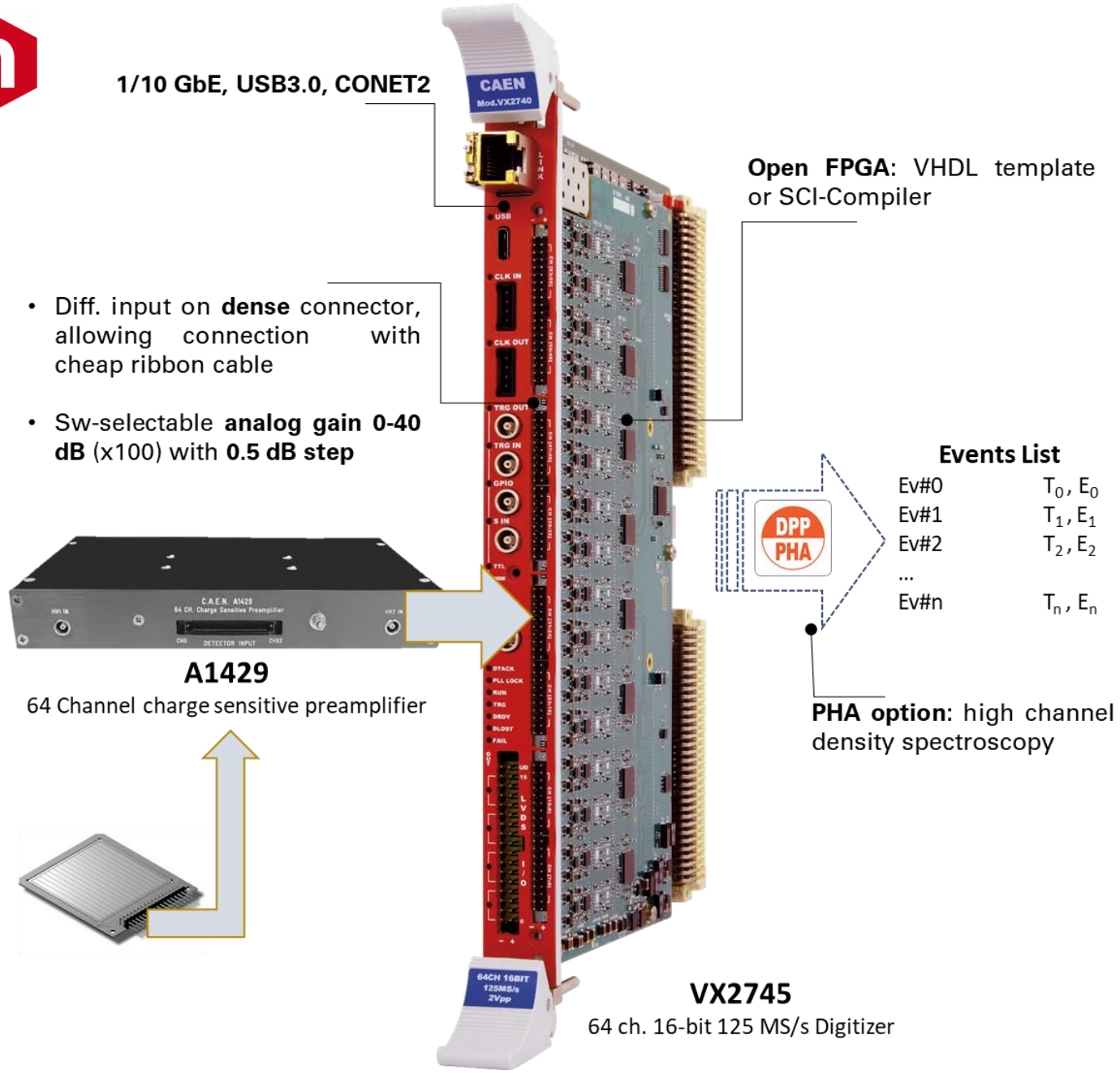
Real Time readout:

- Continuous downstream A/D conversion → Hardware: flash ADC, ASIC-based
- High throughput data transfer → Which communication protocols?
- Buffering and data selection → Which online analysis?
- Event building and DAQ → Integration with which software tools?

New hardware to be flexible

CAEN **always drives to develop** new hardware and to improve its products with new firmware and software tools.

- more channels for denser systems
- faster communication links → high sustainable rate for downstream flow
- from MB to GB on-board memory → storage, middleware running onboard, complex online analysis
- improved FPGA with embedded ARM and OpenFPGA → customizable data processing and selection

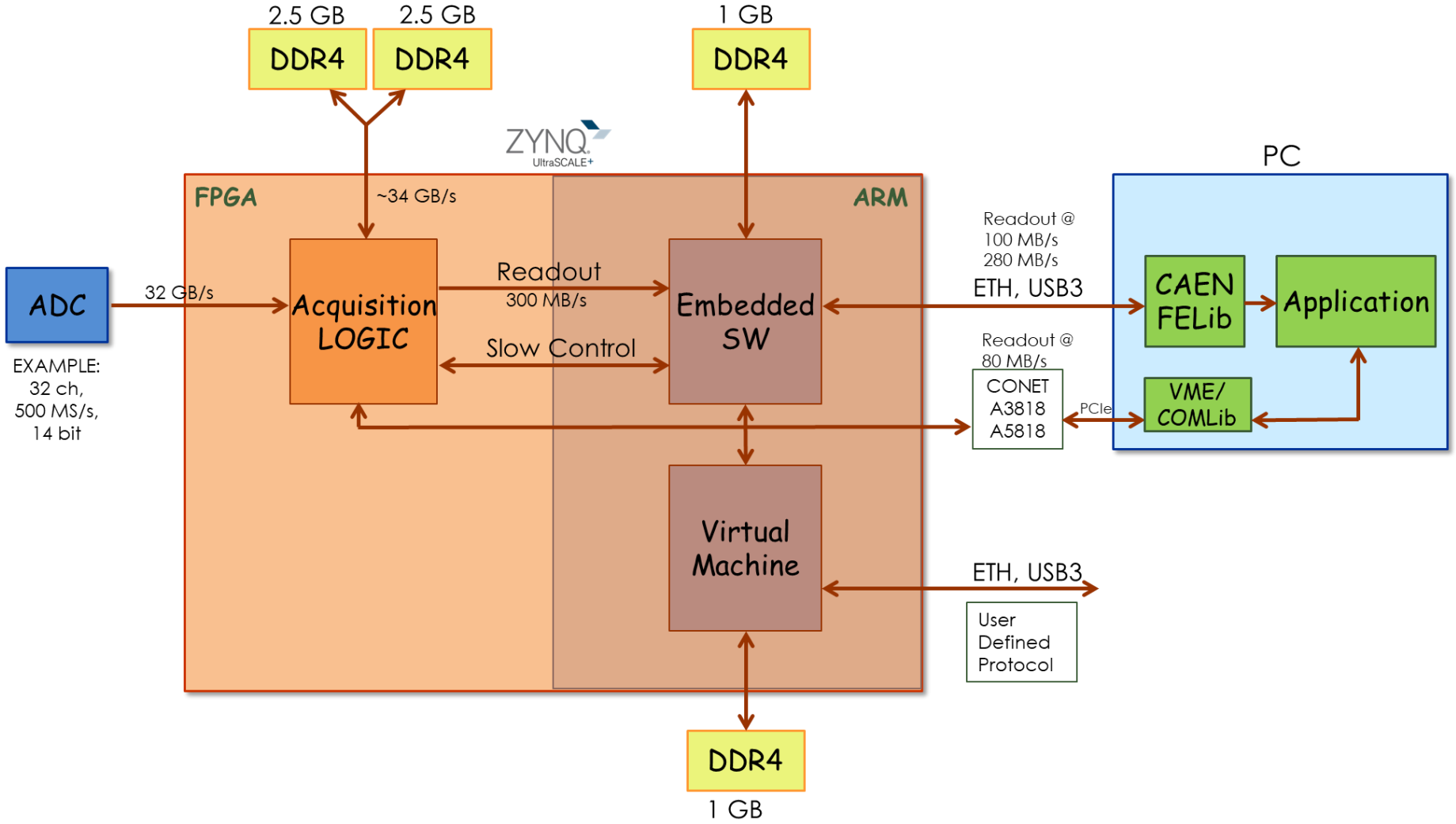


2740/2745 Digitizer

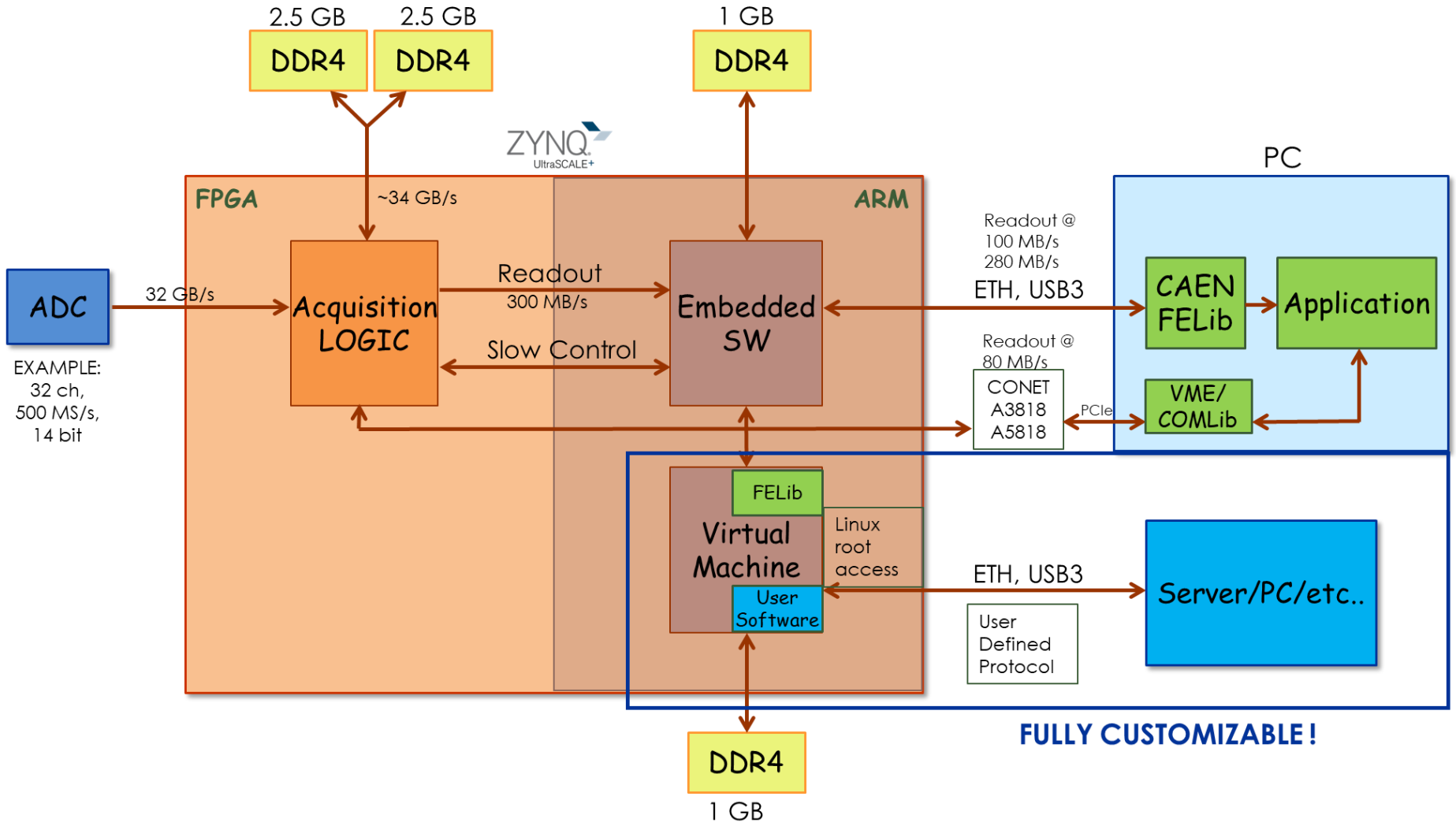
64 channel, 125 MS/s, 16 - bit waveform digitizer

- Good fit for neutrino and dark matter experiments
- Selected by *DarkSide* and *Numen* experiments (SiC, Si-strips, GEMs, Scintillators)
- **Dynamics**: V2740 → 2 V_{pp} fixed , V2745 → 40mV ÷ 4V_{pp}
- Multiple **readout** interfaces
- **Open FPGA** to provide flexibility in the pulse processing algorithm
- DPP functionalities: PHA, QDC, PSD, CFD, Zero Suppression
- Embedded Linux ARM

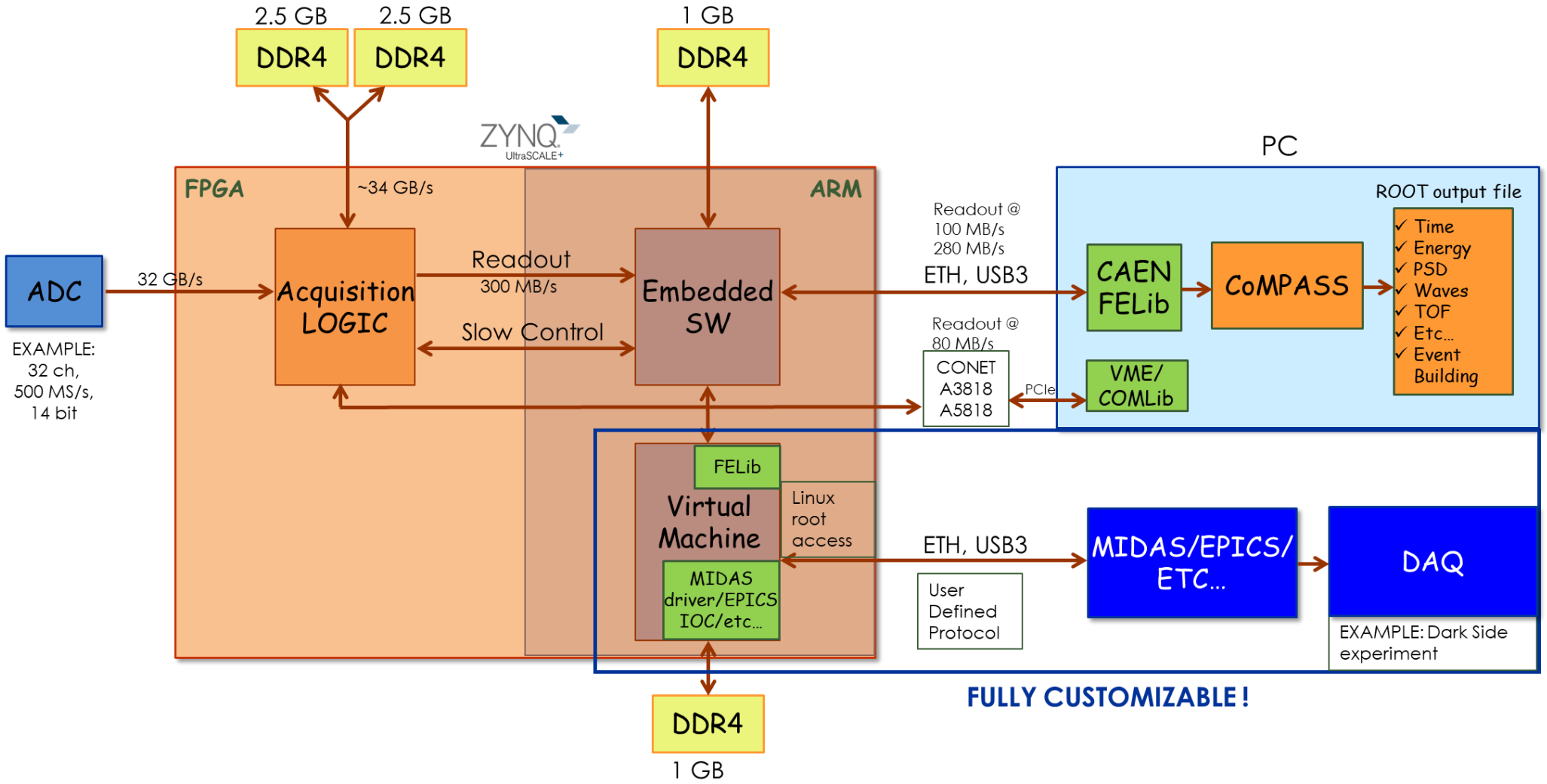
The Digitizer architecture



Focus on the embedded Virtual Machine



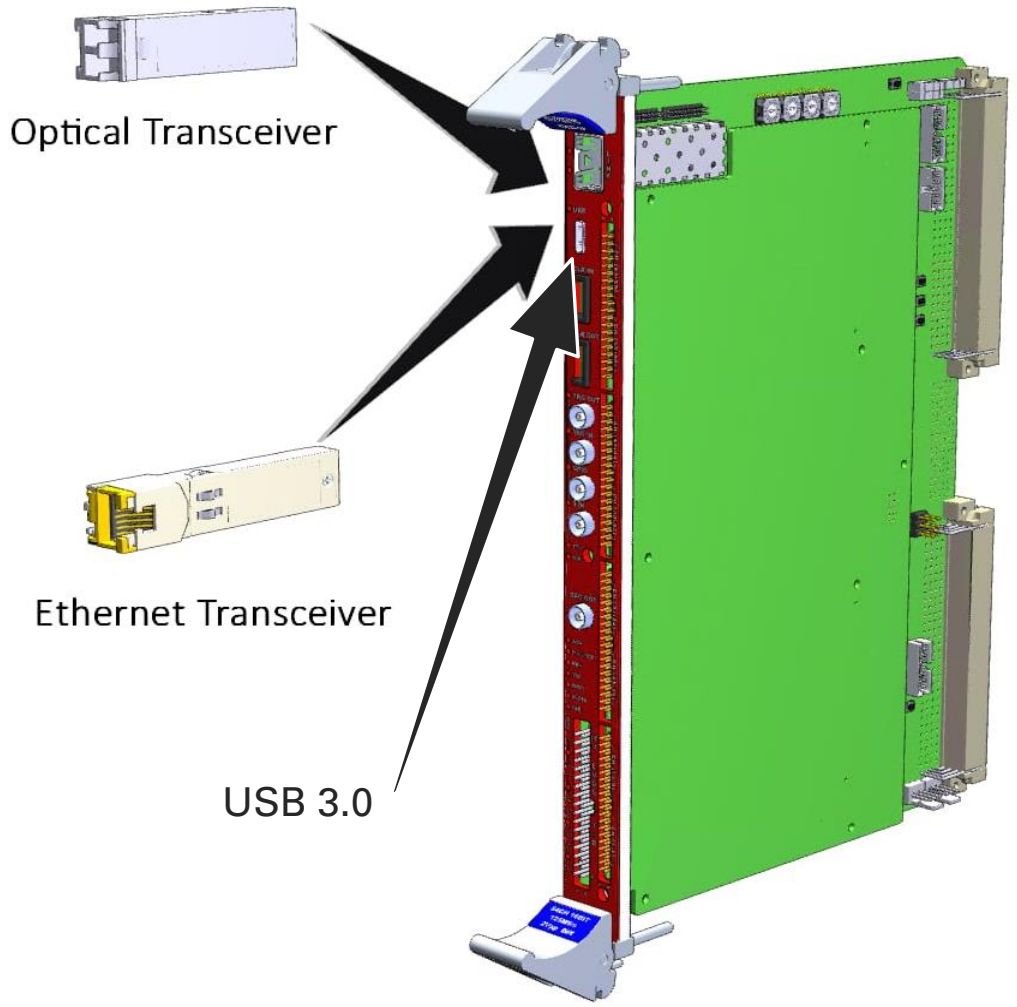
Examples of Applications



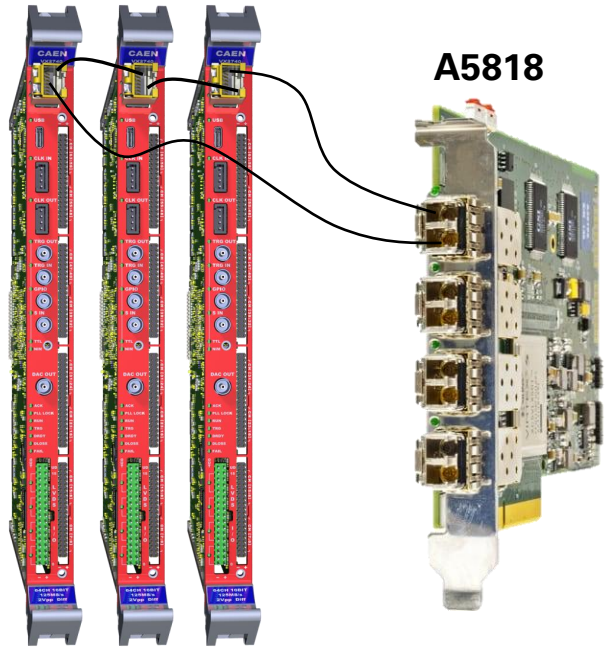
Readout interfaces

- 10 Gb Ethernet: Bandwidth = ~280 MB/s
- 1 Gb Ethernet: Bandwidth = ~100 MB/s
- USB 3.0: Bandwidth = ~280 MB/s
- USB 2.0: Bandwidth = ~30 MB/s
- PCIe: via optical links, daisy chainable.

  Aggregate Bandwidth = ~320 MB/s
- VME: legacy from the past… being dismissed



CONET2/PCIe readout

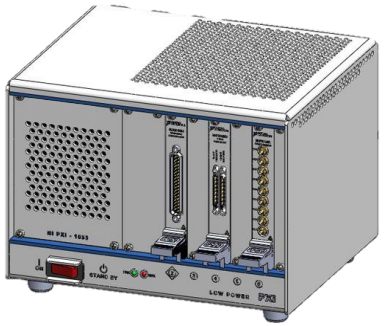


A5818

PC

From VME/VME64x to PCIe

From VME/VME64x to uTCA/PXIe

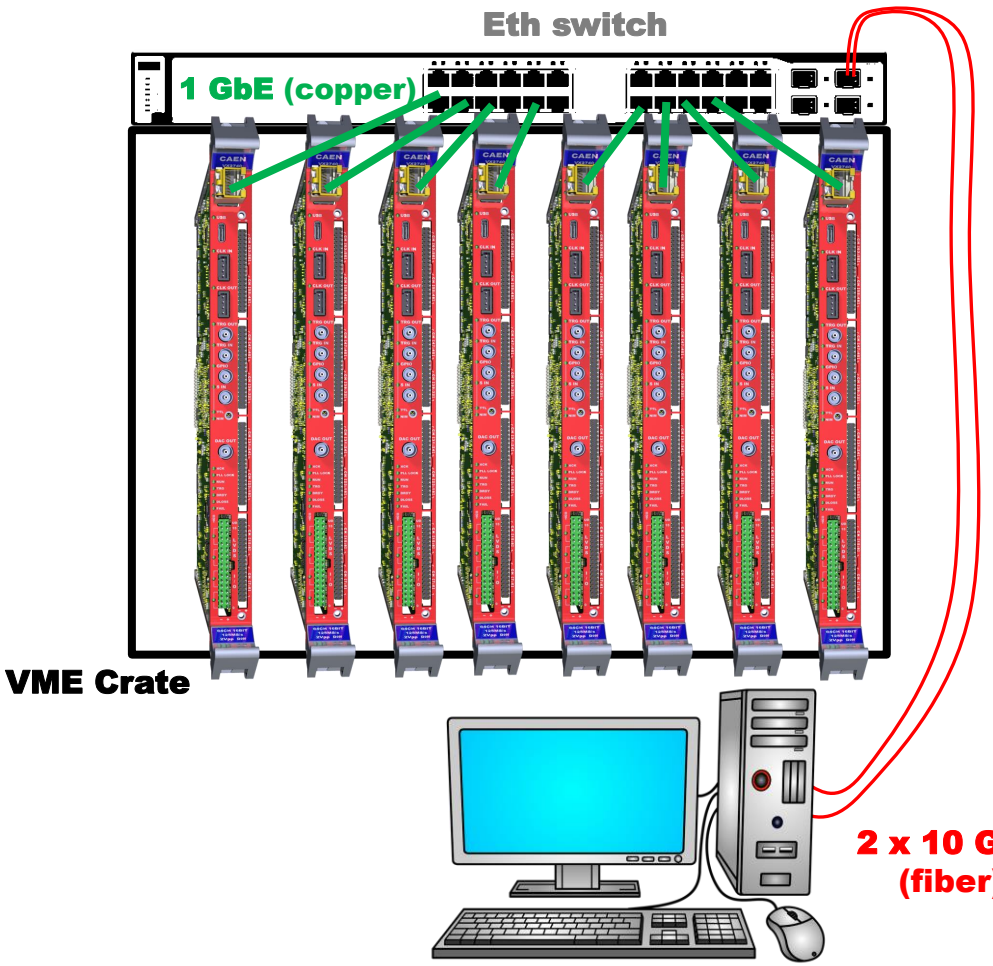


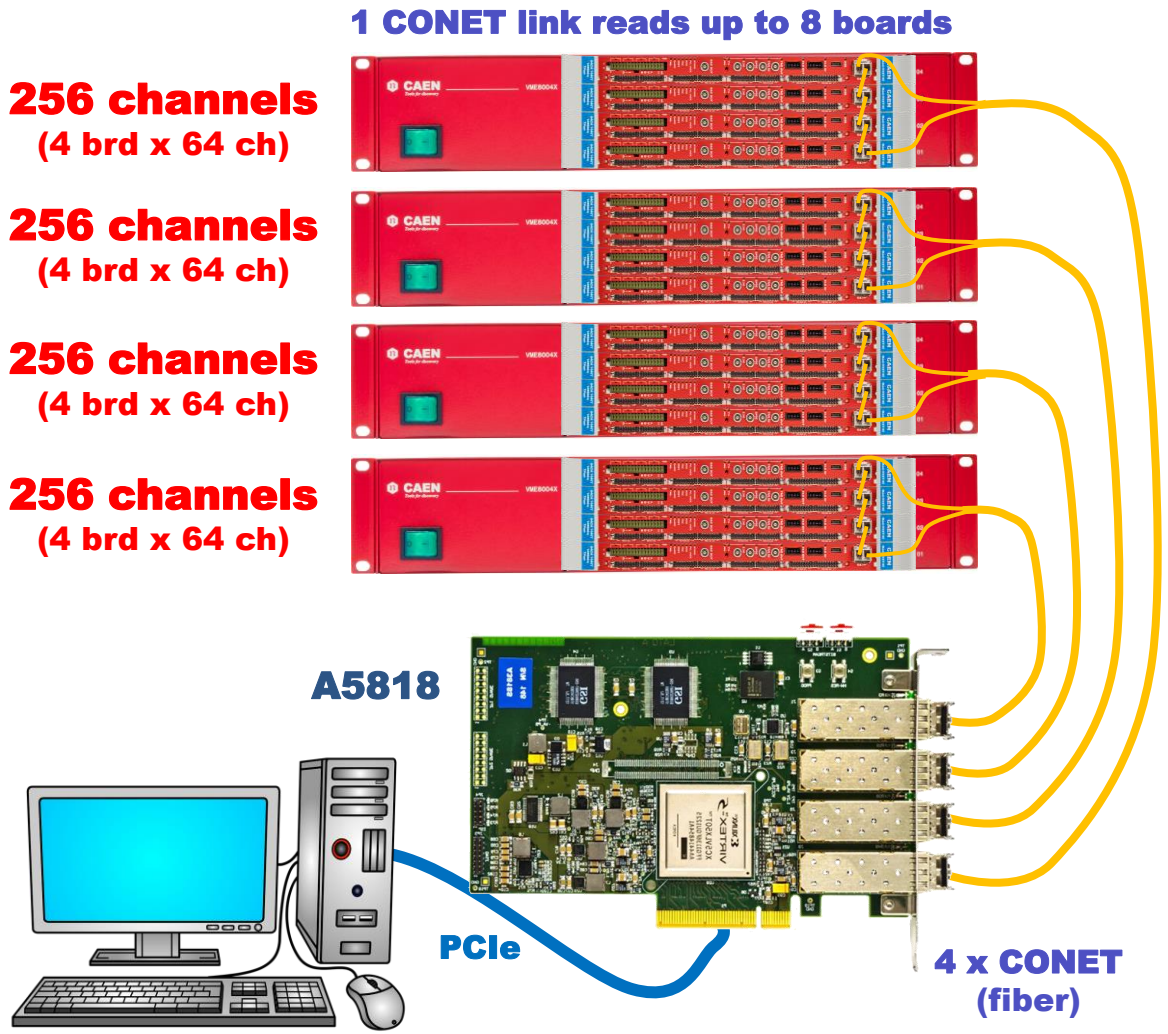
- **Backplane free** policy: VME is kept for power only
- Arrangement in Desktop form factor easily
- A5818 into PCIe slot, but possibility of expansion to uTCA/PXIe

µTCA/PXIe form factor for **A5818.**

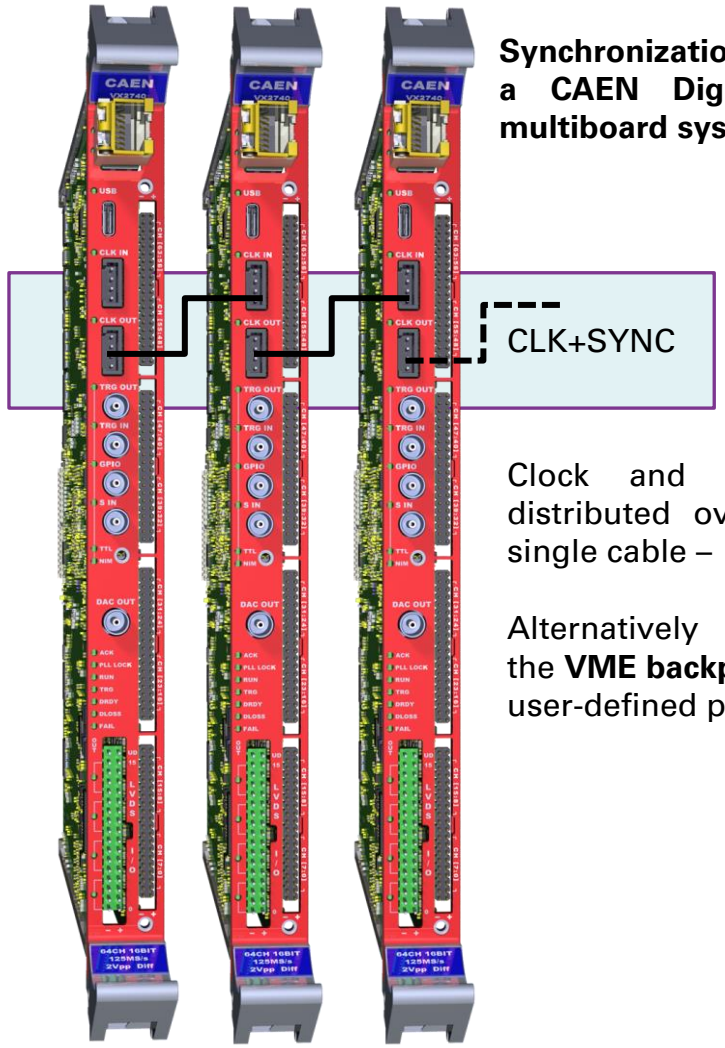
- Cooling
- Size
- PSU quality
- Sophisticated remote monitoring and control

Multiboard Readout – Ethernet vs. CONET2





Digitizers Synchronization



Synchronization of a CAEN Digitizer multiboard system

Clock and Sync distributed over a single cable –

Alternatively over the **VME backplane** user-defined pins

Synchronization with external systems

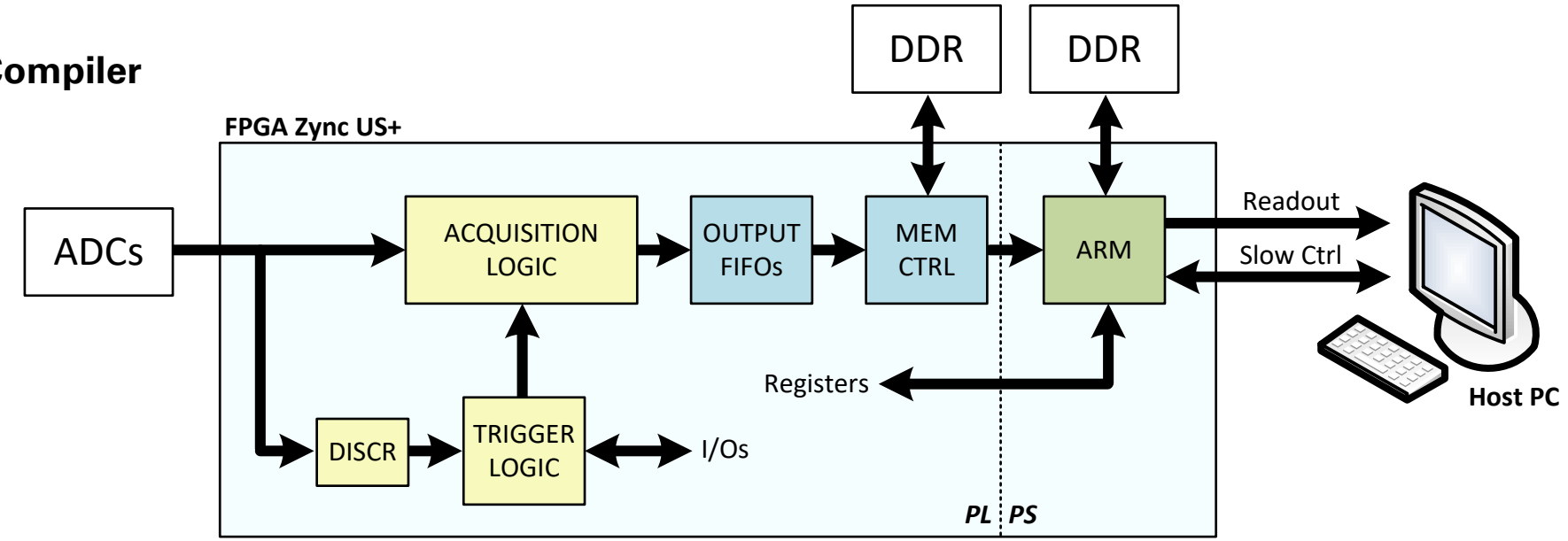
Additional LVDS I/Os for **trigger sharing, busy , veto** and **global timestamp**

Open FPGA

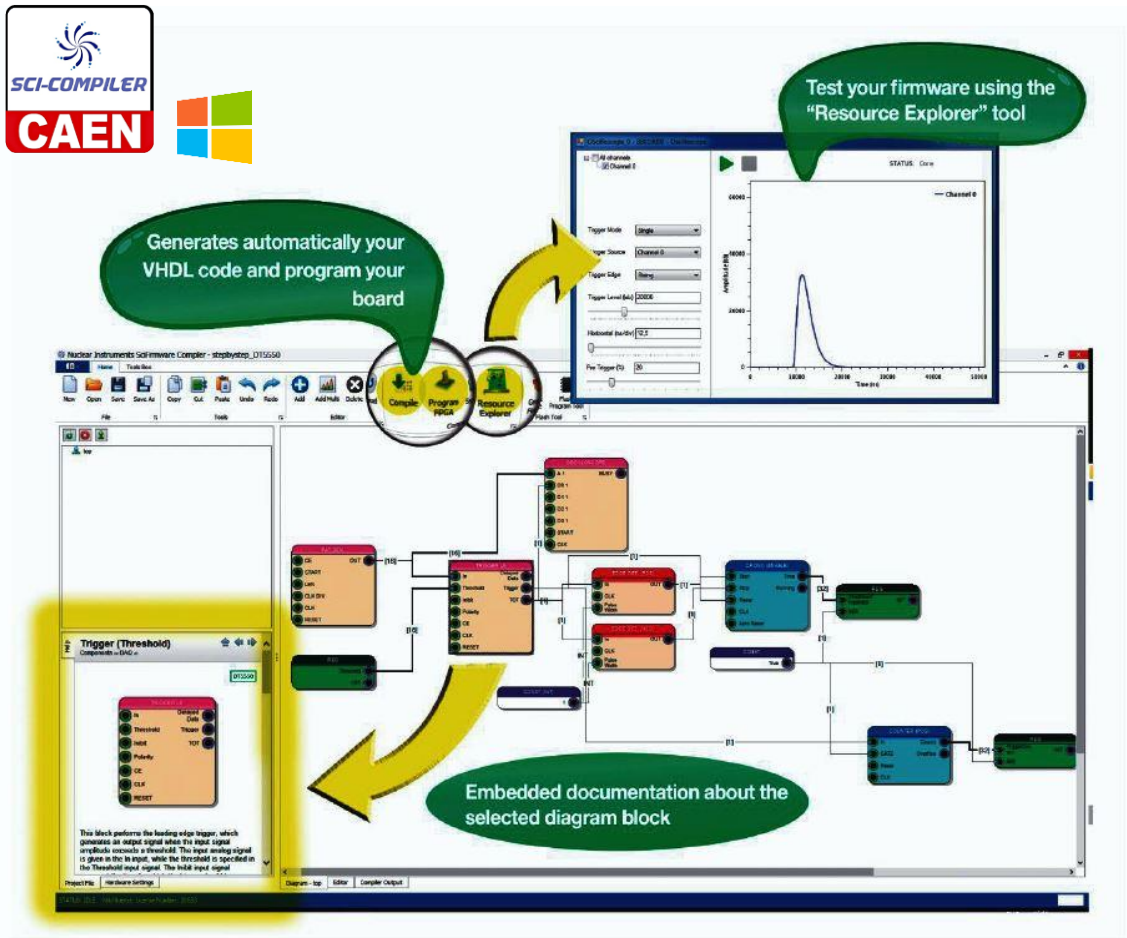
- User can access the **yellow boxes** of the PL to customize Acquisition Logic, Discrimination and Trigger Logic to build **his own Digital Pulse Processing**

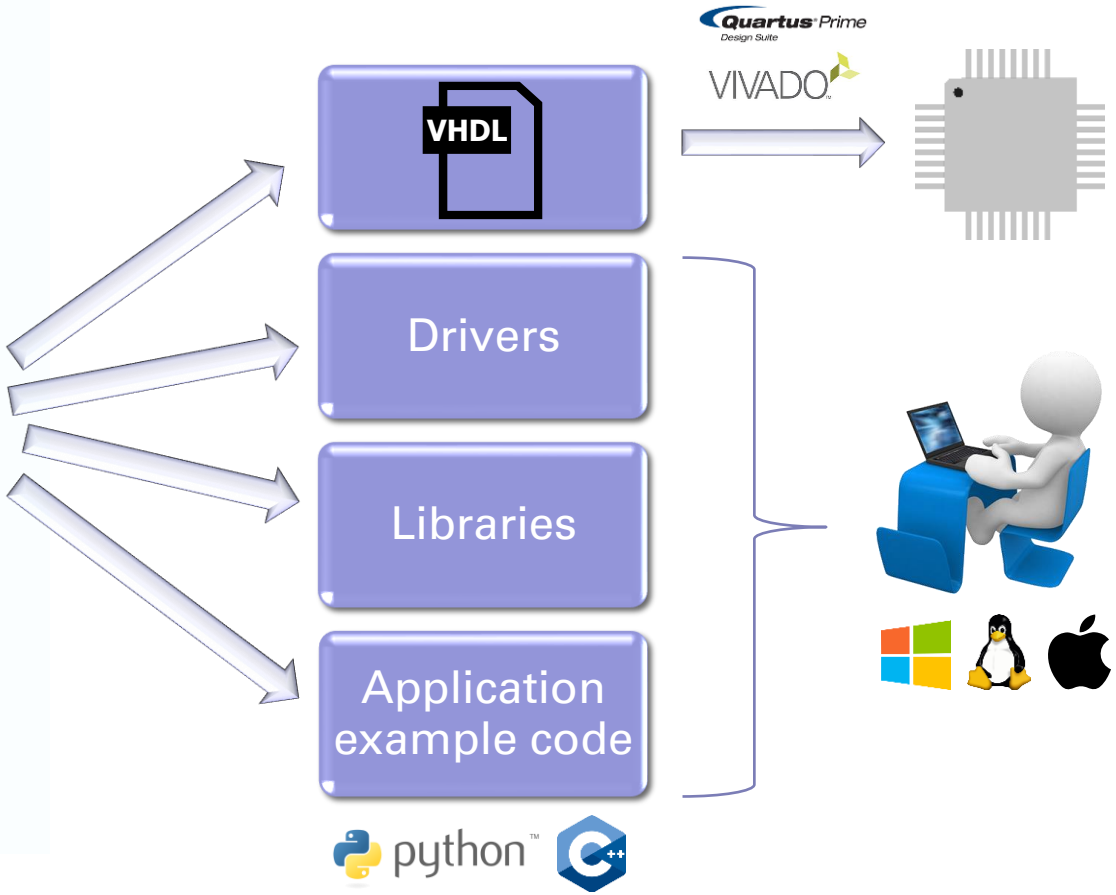
- **FPGA programming:**
  - **Firmware Development Kit** (FDK) , made of a firmware template and VHDL examples – *released upon request to skilled users*

  - **SCI-Compiler**

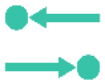


Open FPGA : alternative for transitional R&D





SCI-Compiler: 100+ virtual blocks for physics



I/O INTERFACE

Control Digital and Analog Input/Output of the hardware devices

LOGIC GATE

Coincidence logic, boolean functions, Gate and Delay, counters, timers, scaler, frequency meters, array of bit manipulation

OSCILLOSCOPE

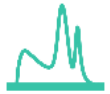
Probe signals of each acquiring channel, even in the middle of the processing chain.

IMAGING

Online image processing capabilities.

TRAPEZOIDAL FILTER

Trapezoidal filter allows to achieve the optimum resolution on HpGE and PMT detectors



ONLINE SPECTRUM

Energy/Time Spectrum can be calculated onboard.

TDC AND TIMESTAMPING

Timestamp events with 0.5 ns resolution and calculate ToT. Digital CFD increase 10x the timing resolution on analog signals

PSD

Pulse Shape Discrimination algorithm to allows for particle identification.

ANALOG SHAPER

High pass and Low pass real-time filter can be combined to emulate a traditional analog shaping chain.

Conclusion

- High throughput data transfer → Which communication protocols?

Several options, we can be standard (GbE, WR ready) or proprietary (CONET, TDLink) – and we can interface with other crate-based protocols like uTCA/PXIe

- Buffering and data selection → Which online analysis?

Open FPGA and ARM gives much flexibility to run custom analysis onboard

- Event building and DAQ → Integration with which software tools?

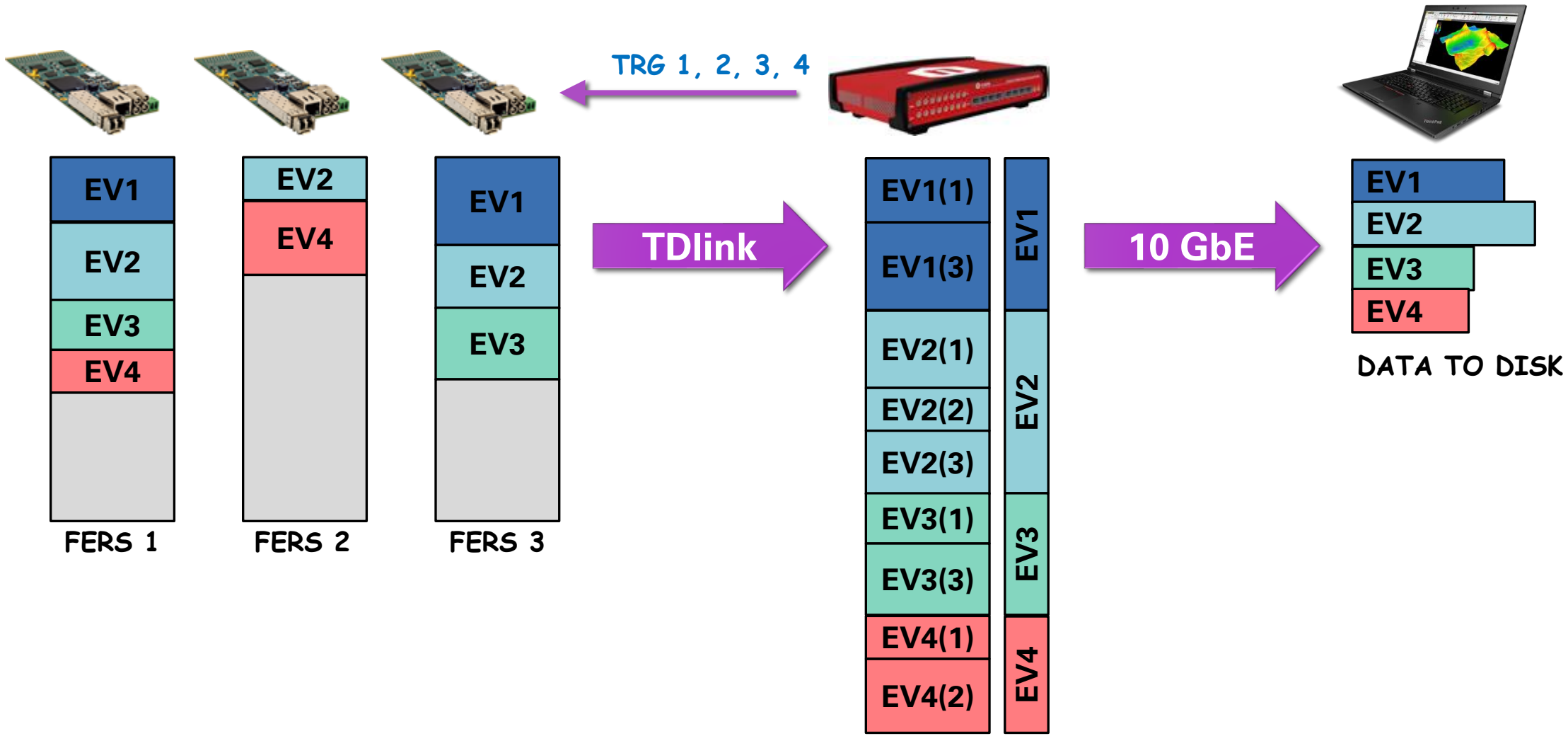
Both new Digitizers and FERS Concentrator Board are ready to handle non-CAEN framework and interface with custom DAQ software

Thank you for your attention

Any question/curiosity?

Backup slides

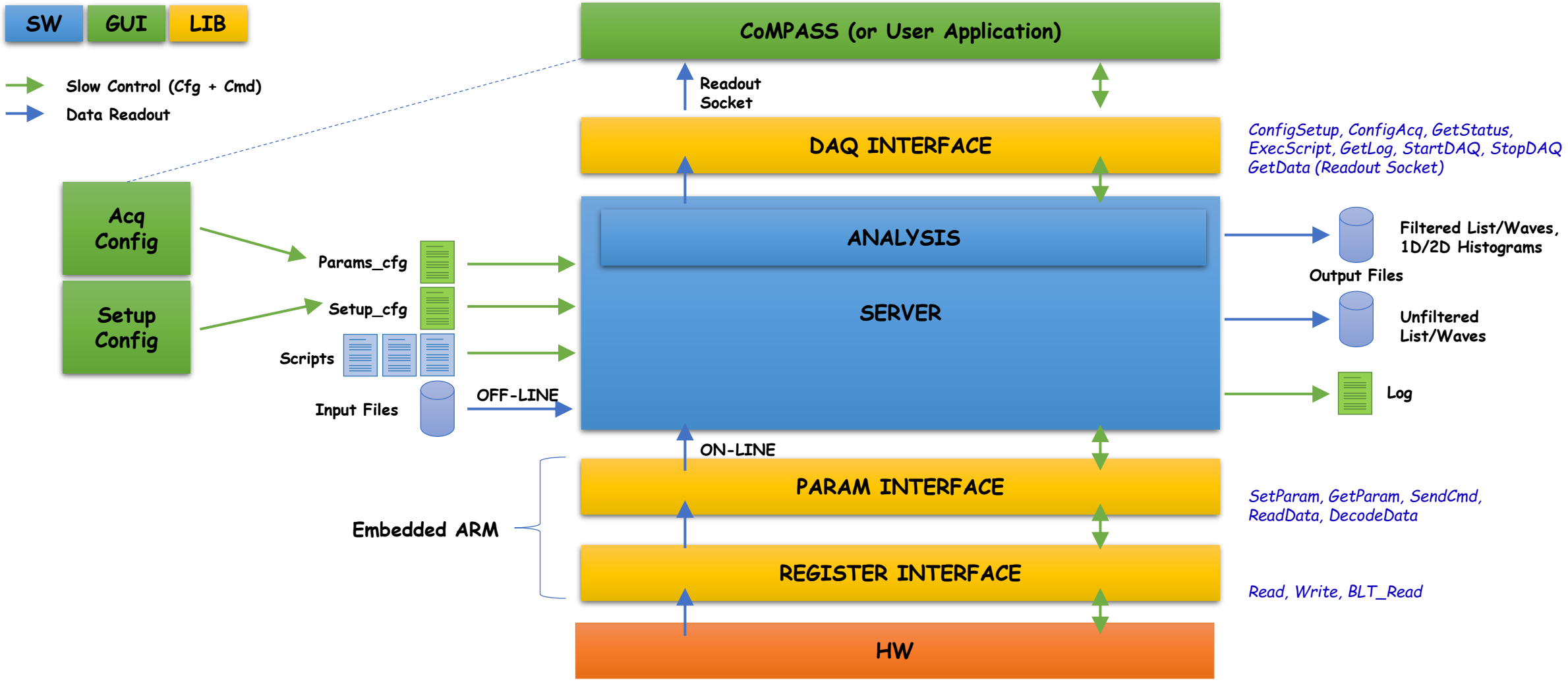
In-built sparse event readout



A5202: readout modes

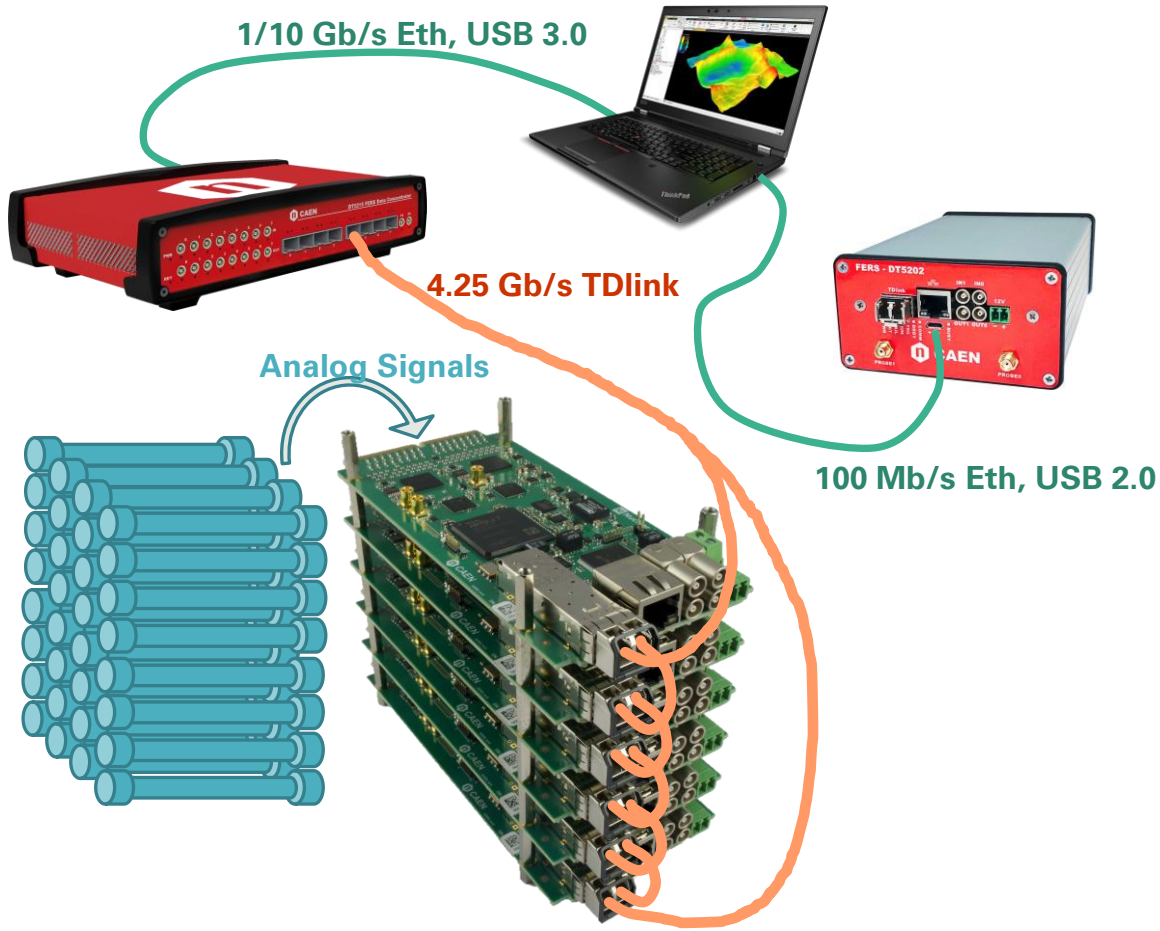
- **Common Trigger Mode**
  - **FERS units**: generate a trigger request (typically OR of channel discriminators)
  - **Data Concentrators**: receive and combine requests from all units and generate the **Global Trigger**
  - **Event Building** and data reduction takes place in the ARM processor of the Data Concentrator
- **Trigger-less Mode (independent channel acquisition)**
  - **FERS units**: each channel pushes data asynchronously, typically at different rates
  - No trigger and data correlation in HW. Events reconstruction in DAQ.
- ARM processor running **Linux** and local DDR memory available in Data Concentrator
- High throughput data transfer to host computers via 10 GbE or USB 3.0
- Users can run custom routines for data handling in the embedded ARM

Software

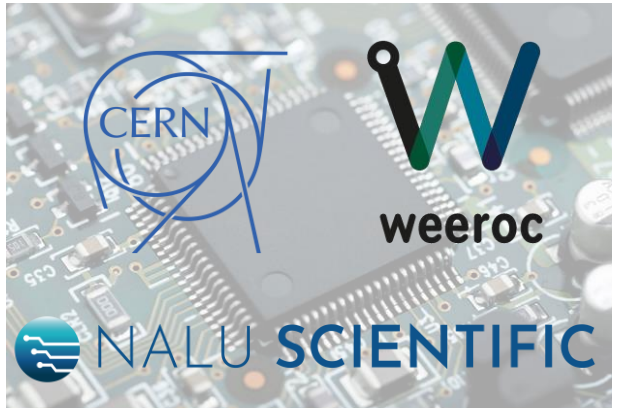


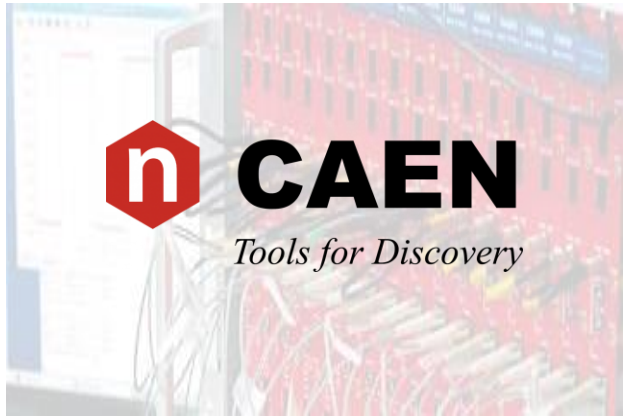
FERS-5200

- **Modular** readout of large arrays of detectors
- **Compact** and **dense** FERS units based on **ASICs**: front-end + digital
- Dedicated protocol developed for **distributed systems**
- **Easy-scalability** of systems through daisy-chain of **fibers**
  1 FERS unit = 64/128 ch
  1 Concentrator = 8k/16k channels
- Stand Alone version for **Evaluation** => scale up to 10k/100k channels with same electronics



Synergies





Off-the-shelf front-end ASIC for scientific instrumentation.

Readout of **SiPMs**, **Si strips**, **GEMs**, PIN diodes, microMegas, MA-PMTs, ... for spectroscopy, PSD, timing applications.

Custom solutions for HEP experiments, with expertise in **rad-hard** design

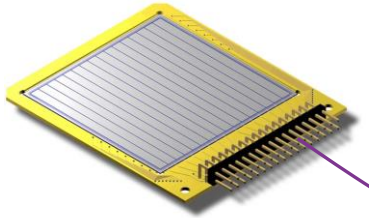
Design of high-end readout electronics and power supply for HEP and NP

We distribute Weeroc worldwide and Nalu Scientific in the U.S. for the scientific community.

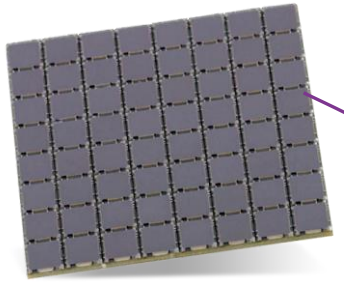
Integration expertise – **FERS-5200** and others

FERS-5200 flexibility

A **compact** and **flexible architecture** supports a wide range of potential applications:

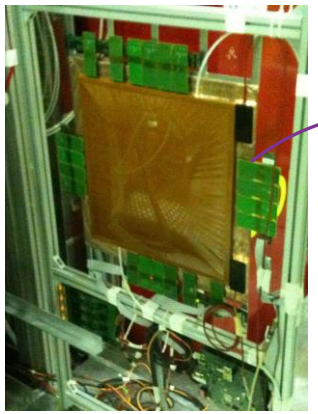


Silicon Strip Detectors



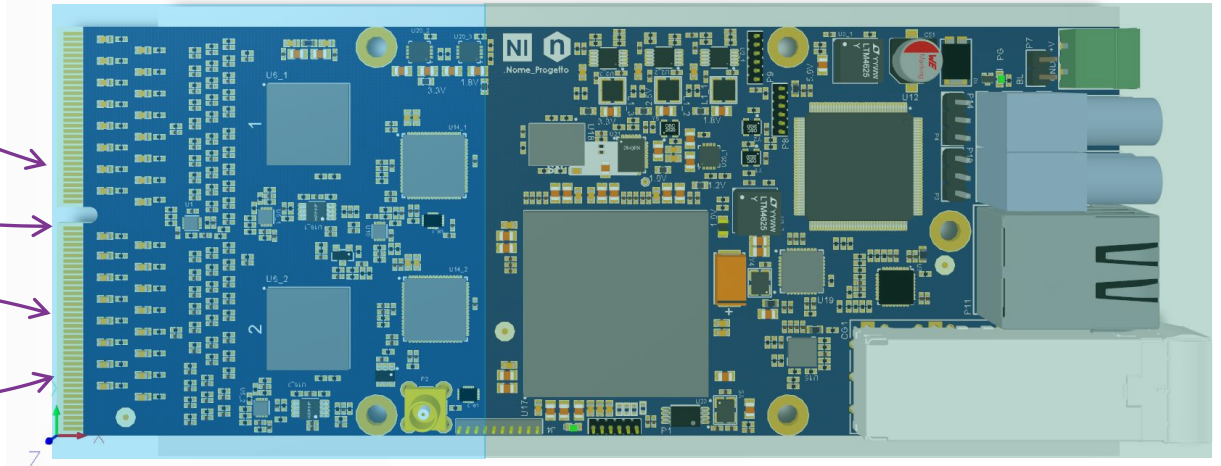
SiPM

Multi- wire chambers



Micromegas, GEMs

Same infrastructure, different Front-Ends by quick integration of different ASICs



DETECTOR SPECIFIC

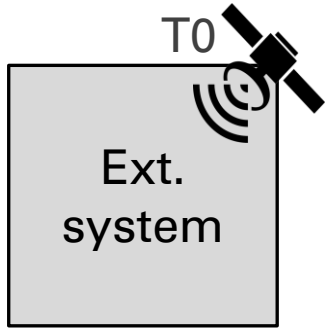
- Weeroc CITIROC - SiPMs
- CERN picoTDC – ps timing
- Weeroc GEMROC - GEMs

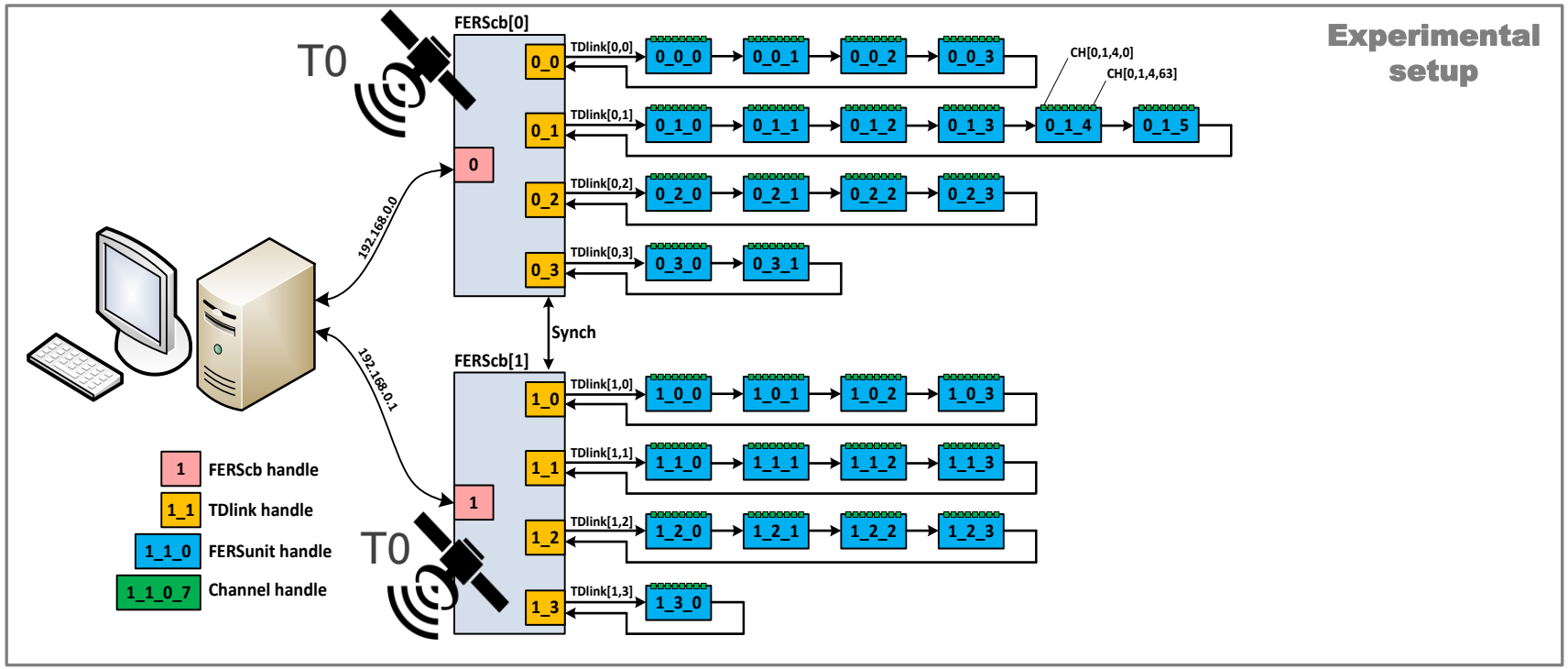
COMMON INFRASTRUCTURE

In the pipeline

TD Link protocol

- **Proprietary protocol TDlink**: 4.25 Gb/s **over fiber** providing *Readout*, *Slow Control*, *Sync* and *Clock* at once
- Allows **alignment of the timestamps with external systems** too – for example GPS



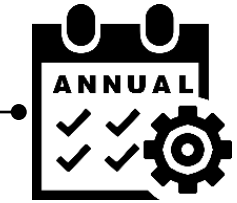


SCI-Compiler: more than a software

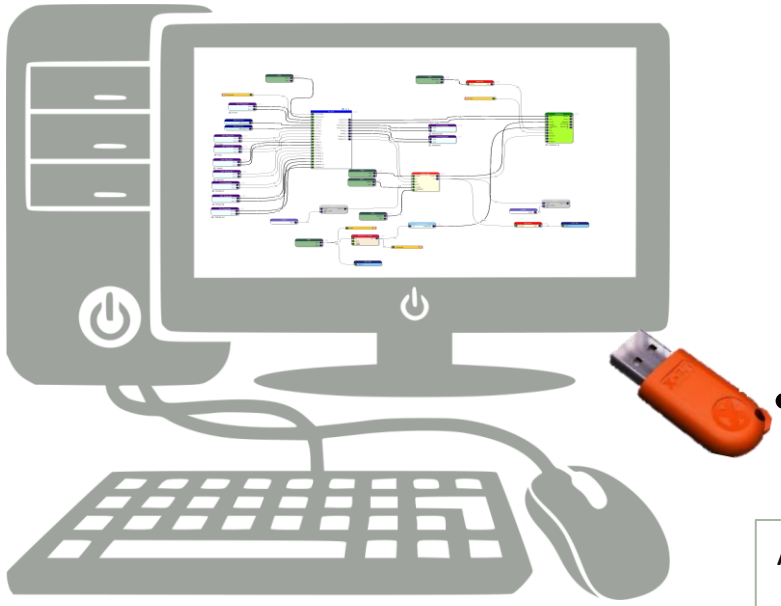
Remote Customization Service

Remote customization service allows to generate the firmware code exploiting the computing power on CAEN server, with **no need of any local FPGA compiler**

Stay **up-to-date** with the newest SCI-Compiler features by subscribing the **yearly upgrade service**



Using a single SCI-Compiler license, it is possible to compile and deploy firmware for **multiple compatible boards** that have been activated through a **runtime license***. A different runtime license is needed for each board.



A **single SCI-Compiler license** can run on a PC relying on a dedicated USB Dongle

*Firmware generated by SCI-Compiler runs for 30-minutes only if no runtime license is installed onboard