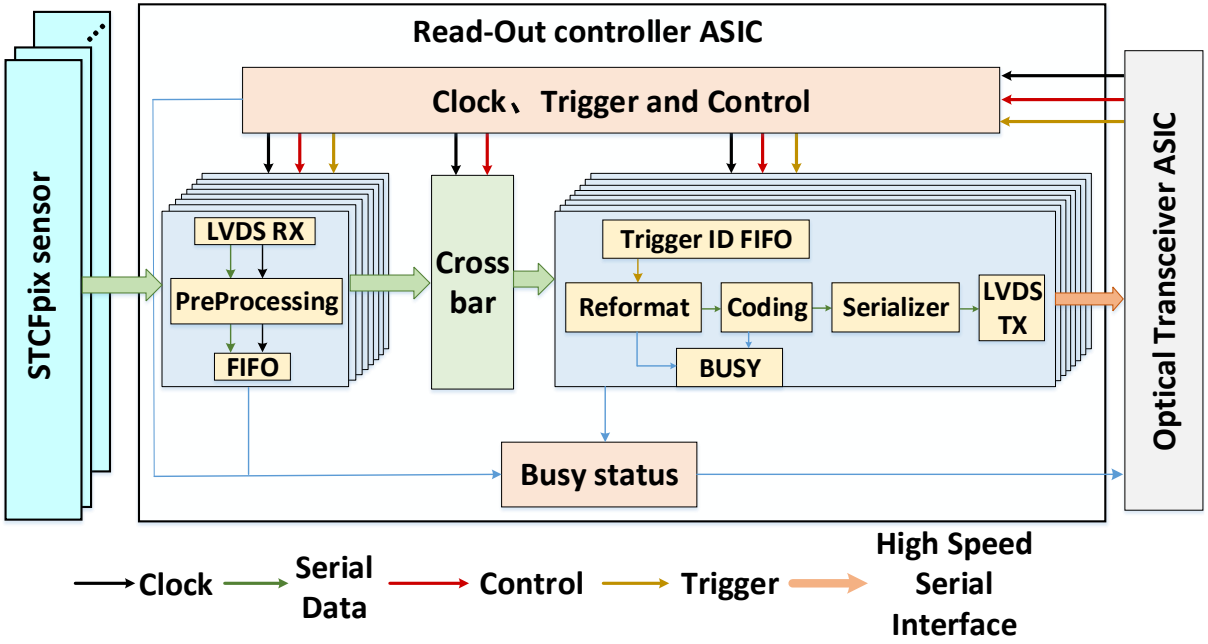
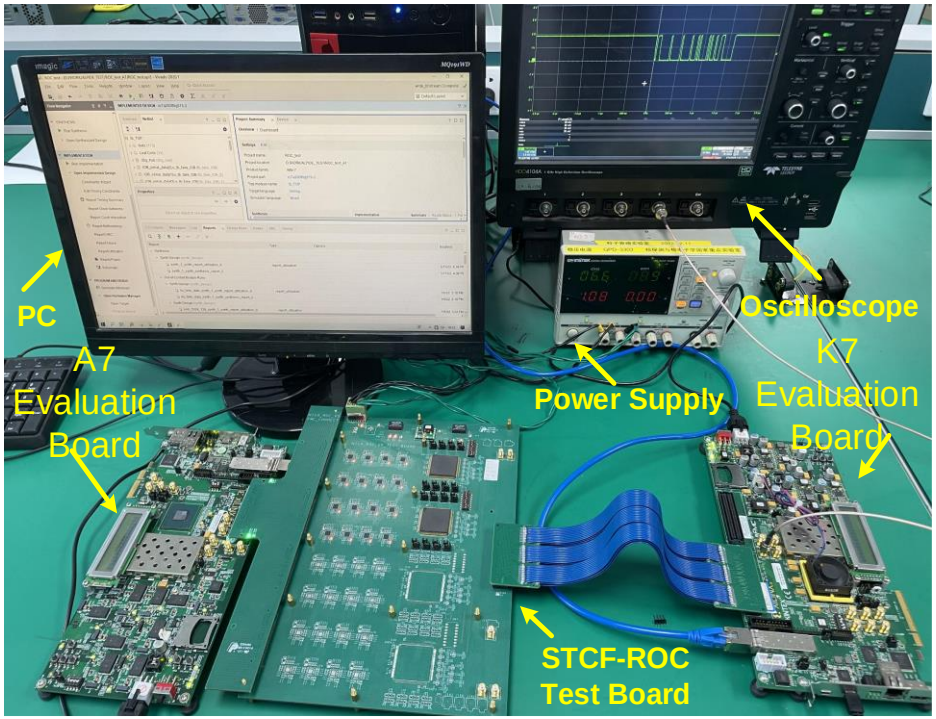
STCF_ROC ASIC Design



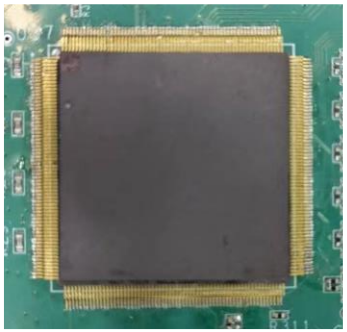
- Design based on a self-defined interface and data format
- Receives trigger/clock/control from STCF_GBT, and distributes the clock and some configure information to the front-end
- Receives the data from ALPIDE modules, aggregates and reformats the data, sends to STCF_GBT

STCF_ROC ASIC

- Use FPGA to simulate MAPS and GBT has all been finished
- The joint test of MAPS and STCF ROC ASIC is in progress

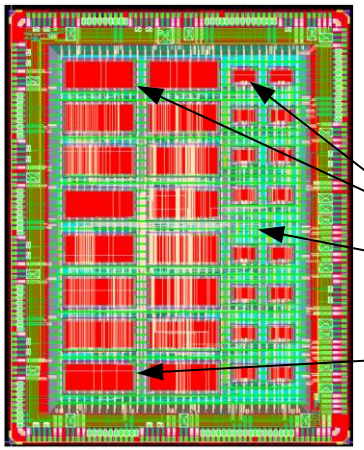


FPGA test system of STCF ROC ASIC



CQFP256
28 mm × 28 mm

STCF ROC ASIC v0



130 nm CMOS
4.4 mm ×5.7 mm

Layout of STCF ROC ASIC