Prototype of a Read-out control ASIC for data collection and commands distribution

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1. Introduction

Super Tau-Charm Facility (STCF) is a High Intensity Electron Positron Accelerator (HIEPA), which is aimed at the spanning center of mass energies ranging from 2 to 7 GeV with the peak luminosity above $0.5 \times 10^{35}\ cm^{-2}s^{-1}$.

STCF Inner Tracker (ITK) is the closest detector to the beam pipe, and improves tracking efficiency at very low momentum. The STCFpix ASIC is being explored for the ITK detector, which contains a matrix of 200×80 sensitive pixels. It provides timestamp, charge, and location information to reconstruct charged particle tracks. The serialized data rate after 8b/10b encoding is up to 400 Mbps. A Read-Out Controller (STCF-ROC) ASIC is designed to concentrate high-speed serial data from multiple STCFpix ASIC. The serial data is filtered, reassembled, and packaged in the ASIC, and then the packaged data are transmitted to gigabit transceiver ASIC through the High-Speed Serial Interface (HSSI). The STCF-ROC also receives control commands, clock, trigger signals from the backend and distributes them to the STCFpix ASICs.

2. DESIGN OF THE STCF-ROC

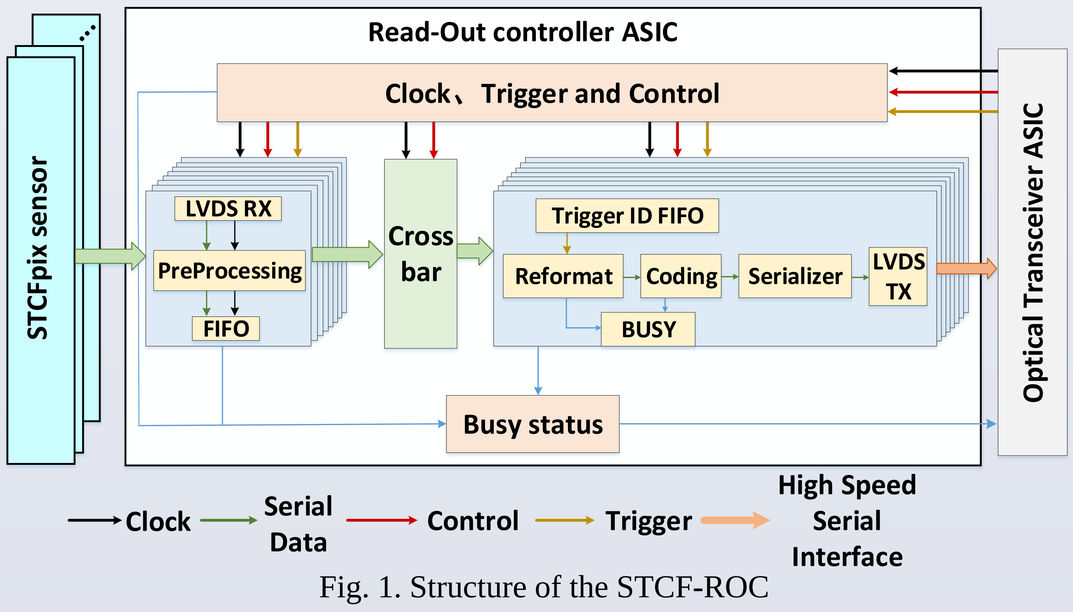

Fig. 1. Structure of the STCF-ROC

A. Structure of the STCF-ROC

As shown in Fig.1, the STCF-ROC contains two links, the uplink contains high-speed stream data and monitoring information to the backend and the downlink is used to distribute control commands, clocks, and trigger signal to the STCFpix ASIC.

The STCF-ROC mainly consists of four modules: serial data preprocessing and cache module, multi-channel crossbar module, data reorganization module, clock, trigger and control (CTC) module.

Serial data preprocessing and cache module to capture the data from the STCFpix ASICs over serial lines, LVDS receiver (RX) to receive serial data at 400Mbps data rate. The preprocessing module converts the serial data to 10-bit parallel data, the parallel data are aligned and decoded. In the preprocessing module, the idle data in the STCFpix ASIC serial data will be removed, and the working state of the CTC module will be adjusted according to the busy information in the data. Preprocessed data are temporarily stored in FIFO.

The multi-channel crossbar module is a fully combinational logic circuit that routes 8 preprocessing modules to 8 reassembly of data modules in a full-mesh network, the selection of the interconnection is determined by the configuration.

According to the configuration, the data reorganization module receives the preprocessed data of multiple channels in a circular manner, and receives Trigger ID from trigger FIFO, start of package, chip ID, and end of package are added to the data packet. Besides, the STCFpix ASIC and STCF- ROC busy status inserted in the data stream (busy-on, busy-off). The coding module encodes the packaged data, and sent out of the chip by a parallel-to-serial conversion module. A 400 Mbps serial data port with differential signaling is the data readout interface.

The CTC module has three main functions. The first is to provide the 40MHz main clock to the STCFpix ASIC. The second is to forward an external trigger signal. The CTC module receives the trigger information and decodes the trigger signal quickly, in different configuration modes, the trigger signal is encoded into a trigger opcode and sent to STCFpix. The CTC module needs to minimize the trigger delay.

The third is to send control commands to the STCFpix and the other modules in STCF-ROC. In order to ensure the accuracy of the configuration information, the control commands sent by the backend includes the Frame Check Sequence. The CTC module verifies the accuracy of the control commands by the CCITT standard 16-bit Cyclic Redundancy Check (CRC), and then decodes the required configuration information.

There will be multiple STCF-ROC ASICs on the readout unit, so STCF-ROC also has the function of transmitting the configuration information.

B. Testbench environment

To ensure the correctness of the STCF-ROC function and timing, we embraced a generic testbench environment consists of input agent, output agent, reference model and scoreboard. Fig.2, shows the STCF-ROC testbench environment.

The input agent block generates virtual data, which simulates the STCFpix sensor output data, the configuration information of the STCF-ROC, as well as the clock, trigger signal, and control commands distributed to STCF pix. and then the virtual data are drives to the STCF-ROC's inputs by a driver.

The virtual data are also sent to the reference model which produces the expected results.

The STCF-ROC's output drives the monitor that takes signal transitions and groups them together into scoreboard block. The scoreboard compares the data from the monitor with those in the reference model.

With the testbench, a large number of test cases are used to verify different working modes and configurations of STCF-ROC, ensuring the completeness of function and timing verification.

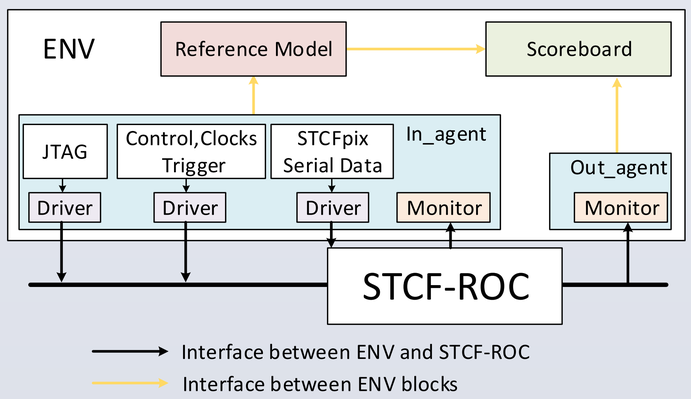

Fig. 2. STCF-ROC testbench environment

3. TEST RESULTS OF THE STCF-ROC

The STCF-ROC chip has been implemented and fabricated in the 130 nm CMOS technology with a 1.2 V supply voltage. Fig.3 shows the Micrograph of the STCF-ROC, the square die has an area of 25 mm^2 and is encapsulated in a 256 CQFP package.

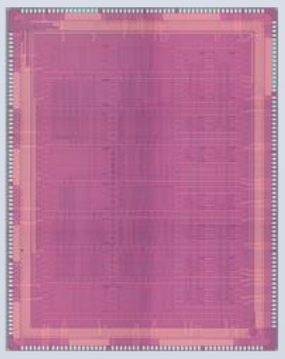

Fig. 3. Micrograph of the STCF-ROC ASIC

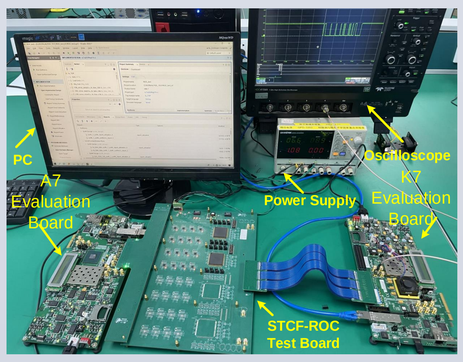

Fig. 4. The STCF-ROC test system

A STCF-ROC ASIC test system, shown in Fig.4, the test board has been designed and fabricated to evaluate the function of the STCF-ROC. Because the STCFpix ASIC is under exploration, the main function of the STCFpix ASIC is simulated by the Xilinx Artix-7(A7) FPGA evaluation board, the Xilinx Kintex-7(K7) FPGA evaluation board receives STCF-ROC output stream data, and provide the control information and clock required by STCF-ROC.

Firstly, the test verifies the decoding function of the configuration information by the CTC module, and the functional correctness is verified by the control commands distributed to STCF. In the K7 evaluation board, compare the STCFpix ASIC virtual data generated by the A7 evaluation board and the STCF-ROC output data, the data processing function under different configuration modes and trigger intervals was verified. The preliminary test results were as expected.