A strip-sensor readout chip for the J-PARC muon g-2/EDM experiment

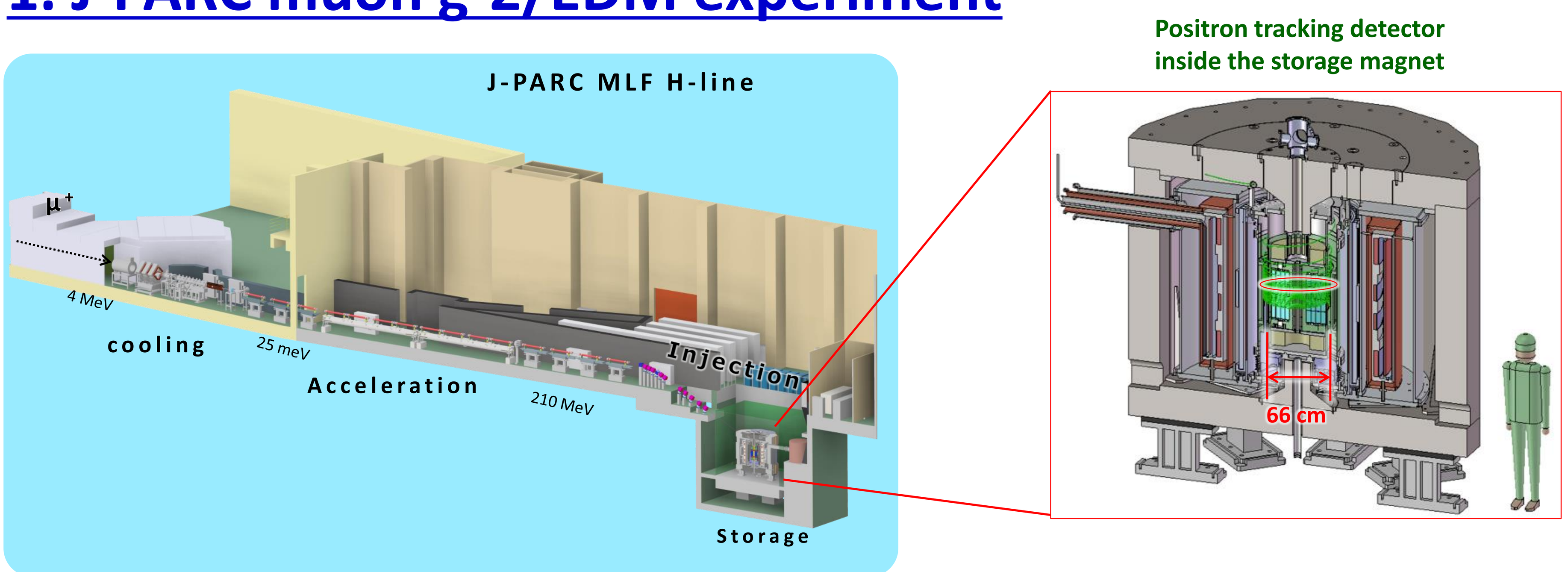
Yutaro Sato[1], Yowichi Fujita[2], Eitaro Hamada[2], Tetsuichi Kishishita[2], Tsutomu Mibe[2], Masayoshi Shoji[2], Taikan Suehara[3], Manobu M. Tanaka[2], Junji Tojo[3], Takashi Yamanaka[3], Tamaki Yoshioka[3] for **the J-PARC muon g-2/EDM collaboration**

Niigata Univ[1], KEK IPNS[2], Kyushu Univ.[3]

Abstract

We have developed a front-end ASIC for silicon-strip detectors of the J-PARC muon g-2/EDM (E34) experiment, which aims to measure the muon anomalous magnetic moment (g-2) and electric dipole moment (EDM) to search for new physics beyond the Standard Model. Since the timing of the muon decay is key information in the experiment, the front-end ASIC is required to tolerate a high hit rate of 1.4 MHz per strip and to be stable to the change of hit rate by a factor of 1/150. To accommodate the pulsed muon beam at J-PARC, the ASIC has large buffer memory to save the binary hit information. "SliT128D" was mass-produced using the Silterra 180-nm CMOS process and performed the operation test. We report the performance of SliT128D chip and future prospect.

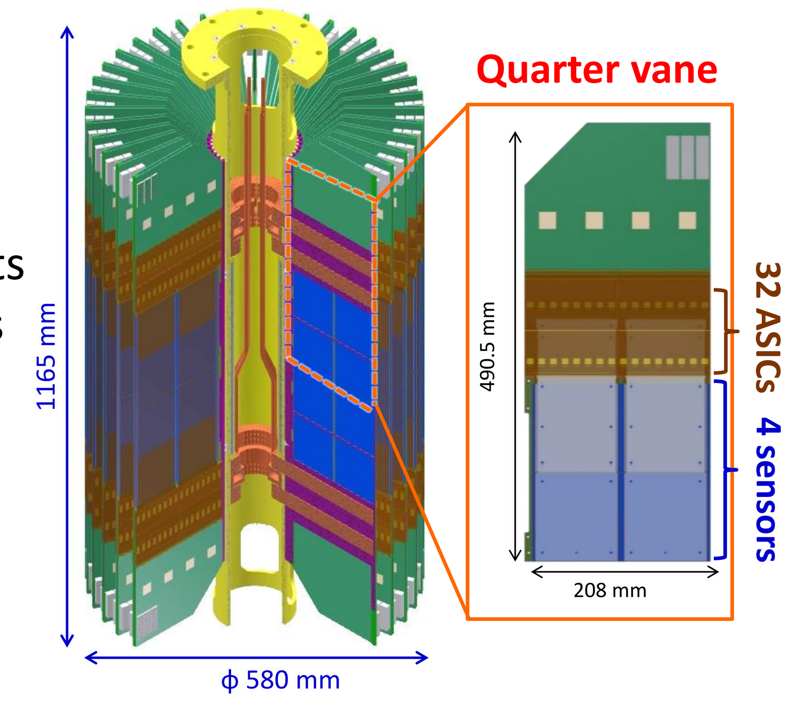
1. J-PARC muon g-2/EDM experiment



- There is 4.2 σ discrepancy between the Standard Model prediction [1] for the muon g-2 and the values measured by the BNL E821 [2] and Fermilab E989 [3].
- J-PARC muon g-2/EDM experiment [4] aims to measure g-2 with a precision of 0.1 ppm and search for EDM with a sensitivity of 10^{-21} e・cm with a different method from BNL E821 and Fermilab E989 experiments.
  - Reaccelerated thermal muon beam with no strong focusing
  - MRI-type storage magnet with a good injection efficiency & high uniformity of local B-field
  - Full-tracking detector with large acceptance

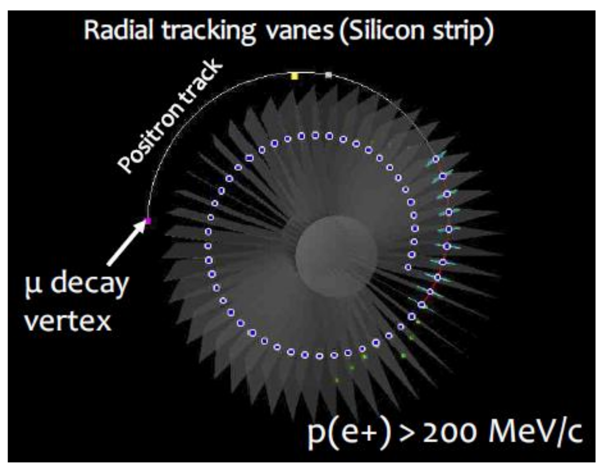
2. Silicon-strip Detector

- Positron tracks from muon decays are measured by silicon-strip detector. It consists of 40 vanes, and one vane consists of 4 quarter-vanes. Each quarter-vane has 4 single-sided silicon strip sensors. Two-dimensional position is measured by the two layers of the silicon strip sensors.
  - 640 sensors
  - 5120 ASICs (=655,360 channels)



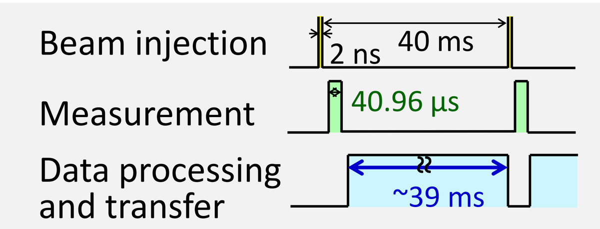
Requirements to detector

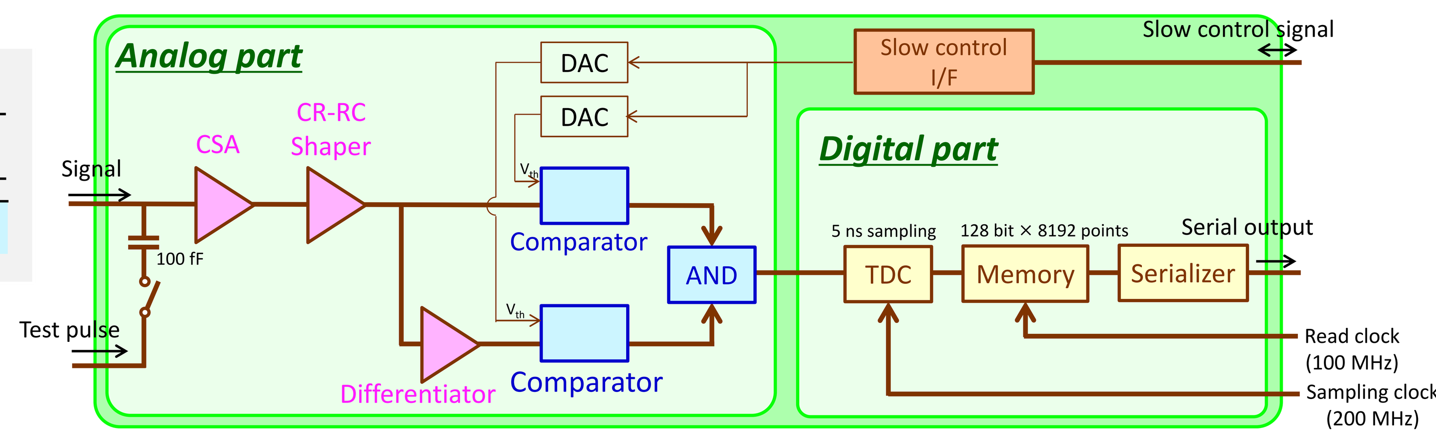
- High tracking efficiency for 100-300 MeV positrons
  - At most 30 muon decays per 5 ns
  - Event rate : 1.4 MHz per strip (max.)
- Stability to hit rate changes
  - Event rate : from 1.4 MHz to 10 kHz per strip.
- Operation in 3T magnetic field and vacuum and no contamination of EM field to the muon storage region.



3. Front-end ASIC "SliT128D"

- Timing stability is important for the measurement of the muon g-2.
  → Fast response to tolerate a high hit rate
- Readout sequence is designed for pulsed muon beam at J-PARC.
  → Binary readout with 5 ns time stamp and larger memory buffer (8,192 depth per channel), in which the data with a period of 40.96 μs can be stored.





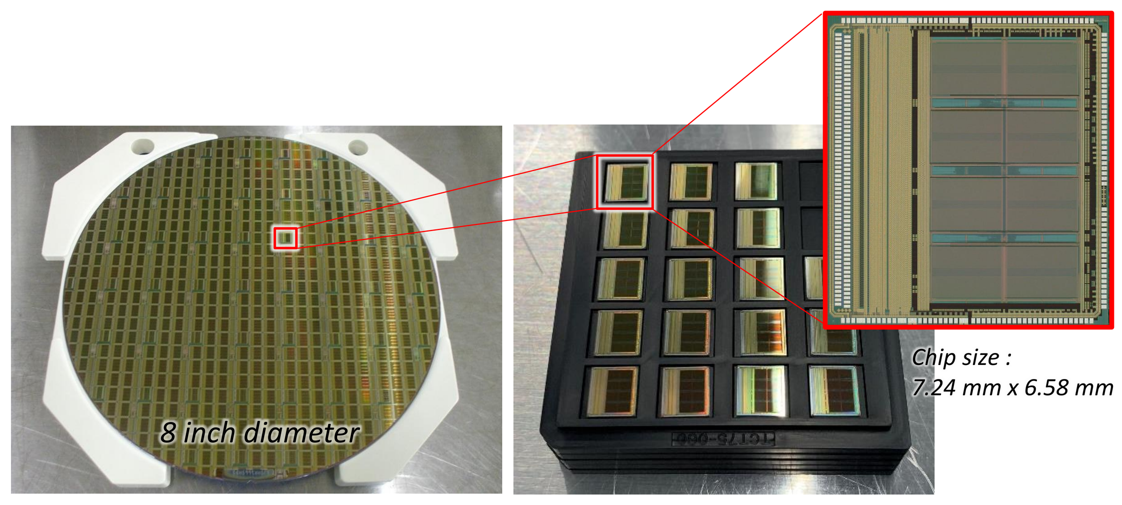
Requirements to ASIC

- Peaking time < 50 ns
- Pulse width < 100 ns
- Dynamic range > 4 MIP (1 MIP = 24,000e)
- Noise : ENC < 1600 e @C_{det} = 30 pF
- Time walk < 1 ns
- Power consumption : 5 mW/ch

History of development of ASIC "SliT"

- 2012 SlitA (16ch, analog) : 1st prototype [5].
- 2013 SlitA2013 (64ch, analog) : the pulse width was improved [6].
  (UMC CMOS 250-nm → Silterra CMOS 180-nm)
- 2015 SliT128A (128ch, analog+digital) : 1st full-scale prototype with analog&digital part [7].
- 2017 SliT2017TEG (64ch, analog) : time-walk was improved by differentiator [8].
- 2018 SliT128B (128ch, analog+digital) :
- 2019 SliT128C (128 ch, analog+digital) : final prototype [9]
- 2020 **SliT128D** (128 ch, analog+digital) : mass-production ← **report in this poster**

- Mass production of the "SliT128D" was successfully completed.
- 5,120 chips (+ spares) are needed for full-detector (40 vanes).
- After the wafer dicing, more than 15,000 chips were obtained from 37 silicon wafers.
  - Yield of wafer dicing > 99%.

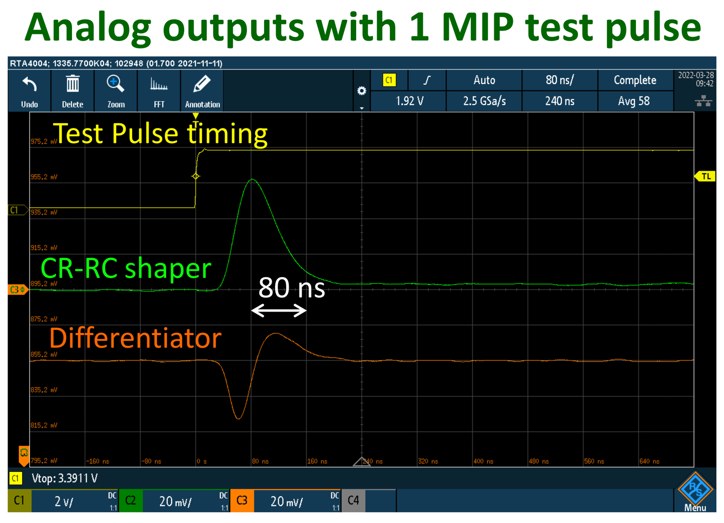


4. Performance Test

Peaking time and pulse width

- All analog outputs are observed through monitor lines.
- Peaking time ~ 50 ns & pulse width ~ 100 ns. ☺
  - Output measured from the monitor which include delays due to the parasitic capacitance and finite buffer drive strength

Analog outputs with 1 MIP test pulse

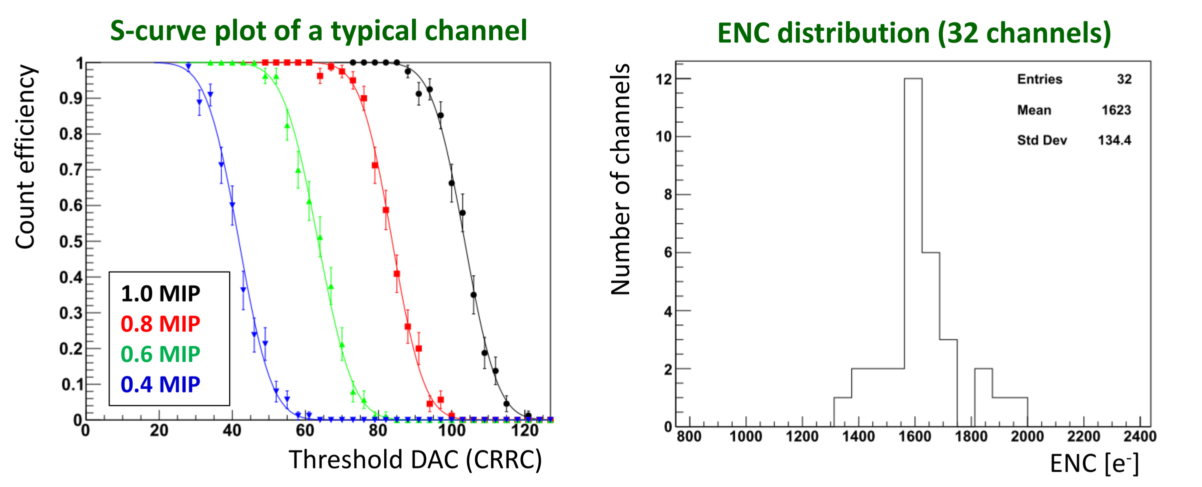


Power consumption

- Power consumption is estimated to be 0.32 W, which is less than the requirement (< 0.64W/chip). ☺

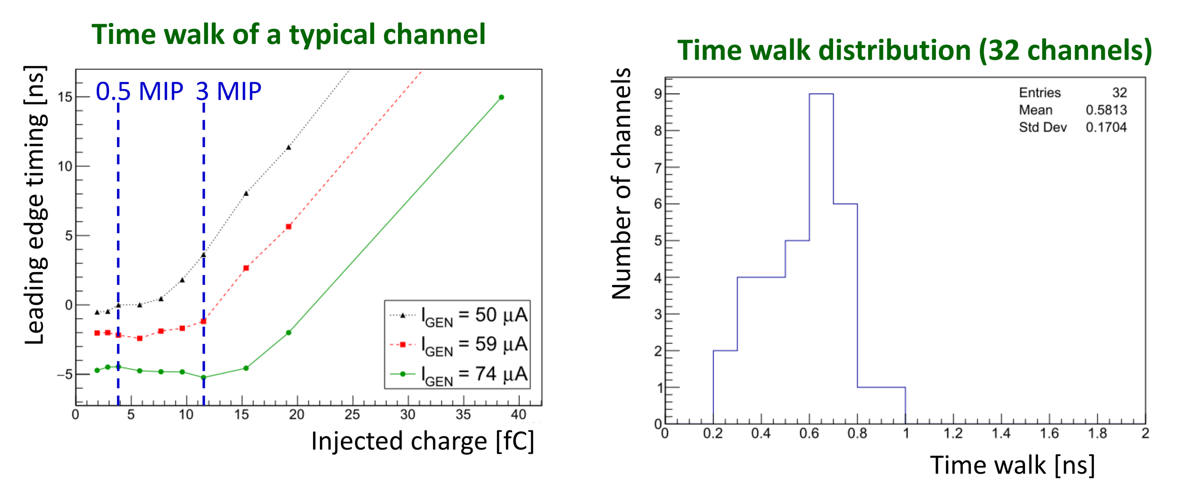
Noise

- "S-curve scan" is performed to estimate the noise.
  - A fixed amount of charge is injected, changing the threshold voltage of comparator.
  - Response function is error function, which is step function smeared by noise.
- ENC is estimated to be (1,627 ± 23) e^- with C_{det} = 33 pF.
  - ➢ ENC = (1,534 ± 23 e^-) with C_{det} = 30 pF ☺
    (requirement < 1600 e^-)



Time-walk

- Time-walk is defined as the maximum time difference between 0.5 and 3 MIP.
- The time walk effect on the large injected charge can be reduced by increasing the reference current (I_{GEN}) for the CR-RC shaper.
- All measured channels have time walk less than 1 ns (requirements).
  - Average time walk = (0.58 ± 0.17) ns ☺



5. Summary and Prospect

- Front-end ASIC "SliT128D" for J-PARC muon g-2/EDM experiment were mass-produced.
  - Fast response, small time walk effect, binary output with 5 ns time stumps, large memory buffer (8,192 depth per channel)
- QA (quality assurance) system for the SliT128D is being developed.
- Detector module will be assembled with the chips after QA.

References

[1] T. Aoyama et al, "The anomalous magnetic moment of the muon in the Standard Model", Phys. Rep. 887 , 1 (2020)
[2] G.W. Bennett et al, "Final report of the E821 muon anomalous magnetic moment measurement at BNL", PRD 73, 072003 (2006)
[3] B. Abi et al, "Measurement of the Positive Muon Anomalous Magnetic Moment to 0.46 ppm", PRL 126 14, 141801 (2021)
[4] M. Abe et al., "A new approach for measuring the muon anomalous magnetic moment and electric dipole moment", PTEP 2019, 053C02 (2019)
[5] K. Ueno, et al., "Fast Readout ASIC for Si-Strip Detector in the J-PARC Muon g-2/EDM Experiment and Other Related Applications", IEEE NSS/MIC Conference (2013), NPO2-220
[6] S. Shirabe, et al., "An Improved Fast Readout ASIC for Si-Strip Detector in the J-PARC muon g-2/EDM experiment and Other Related Applications", IEEE NSS/MIC/ Conference (2014), N03-15.
[7] Y. Sato et al., "Performance of Front-end ASIC and its evaluation with Silicon Strip Sensor for J-PARC Muon g-2/EDM Experiment", IEEE NSS/MIC Conference (2017), doi: 10.1109/NSSMIC.2017.8532754
[8] Y. Tsutsumi et al., "Prototype Front-end ASIC for Silicon-strip Detectors of J-PARC Muon g-2/EDM Experiment", PoS(TWEPP2018)090
[9] T. Kishishita et al., "SliT: A Strip-sensor Readout Chip with Subnanosecond Time-walk for the J-PARC Muon g-2/EDM Experiment", IEEE Trans. Nucl. Sci. 67, 2089 (2020)

Yutaro Sato (Niigata Univ.) Email:syutaro@post.kek.jp