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The Design of Low-Jitter Delay-Locked Loop for Ultra High-Resolution Time Measurement

This work is the demand for the fixed and low-jitter delay generation circuit in the time measurement system. As the timing resolution required by modern electronic products constantly improve, the multi-phase clock sampler and the vernier delay line have become frequently-used structures of the ultra-high-resolution time-to-digital converter (TDC), which are both implemented with the fix delay provided by the delay-locked loop (DLL). This work presents a low-jitter and small-static-phase-error DLL, which is composed of an incorrect lock prevention circuit, a phase detector, a charge pump, a voltage-controlled delay line and auxiliary circuits. The proposed charge pump in this work is equipped with the wide-swing cascode current mirror, the clamping amplifier and the virtual switch to eliminate the influence of non-ideal effects. A new current-starving delay cell is also proposed to expand the adjustable range of the control voltage. The proposed DLL is designed and fabricated with standard 180 nm CMOS process. According to simulation results with 100MHz reference clock, this DLL can get the rms jitter better than 15 ps and the static phase error better than 40 ps. The power consumption of the overall circuit is about 3.3mW.

Minioral

No

IEEE Member

No

Are you a student?

Yes

Authors: FENG, Miaohui (Northwestern Polytechnical University); ZHAO, Ziwei (Northwestern Polytechnical University); WEI, Xiaomin (Northwestern Polytechnical University); WANG, Jia (Northwestern Polytechnical University); ZHENG, Ran (Northwestern Polytechnical University); XUE, Feifei (Northwestern Polytechnical University); HU, Yann (Northwestern Polytechnical University)

Presenter: FENG, Miaohui (Northwestern Polytechnical University)

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