23rd Virtual IEEE Real Time Conference

Triggerless Electronics based on HTM Method for Cosmic Ray Muon Imaging

Nan Li[1], Jianing Dong[1], Haifeng Li[1], Qingchen Li[1], Xiangxiang Ren[*,1]

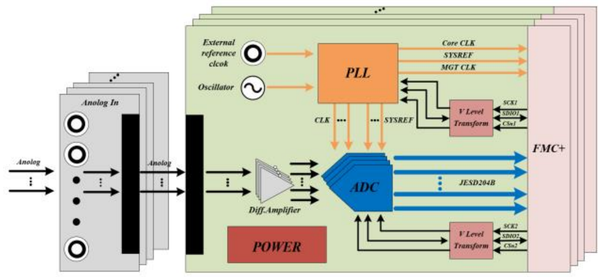
[1]Shandong University, Qingdao 266237, China *renxx@sdu.edu.cn

Abstract

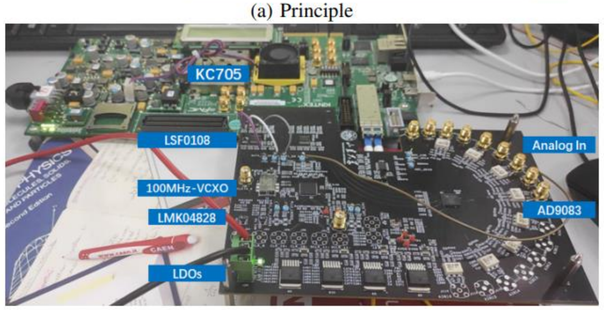
The optical scintillation fiber detector designed for muon imaging usually requires thousands of electronic readout channels, for this reason, a set of trigger-less multi-board synchronous data acquisition(DAQ) system is designed, its single board Analog-to-Digital Converter(ADC) can carry four 64 channel sigma delta ADC, in which oversampling method and the embedded digital shaping and filtering module help to better reconstruct the analog signal. The digitized signal is received by Field Programmable Gate Array(FPGA) which then interacts with server. In order to solve the problem of multi-board synchronization, for the digital front-end part, the clock board is designed to provide the homologous clock for the whole DAQ system. For the back-end, the data packet is split with Head-Tail Marking(HTM) method on the server to realize data synchronization. In Pandax-4T experiment, due to the large bandwidth input of signal source, there is congestion when calling memory on the server side to receive and sort data packets. Here, correction will be added on the FPGA to reduce the size of data packets with HTM method and reduce the memory call pressure of the server, and realize the multi-board synchronization of the system.

DAQ system design

The digitized part of DAQ system is shown in Fig.1. The selected digitizer is ADI product AD9083. The sampling rate is up to 2 GSPS. It supports 16 channel analog signal input at most, the input bandwidth is up to 125MHz and the data output rate is up to 16 Gbps per lane. The clock source supports both on-board crystal oscillator and external clock input. The PLL, for clock jitter clean and frequency division, selects ultra low noise JESD204B compliant clock jitter cleaner, LMK04828 designed by TI.



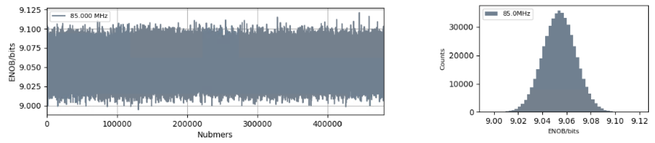
(a) Principle



(b) Test board

Fig. 1: The digitized part of DAQ

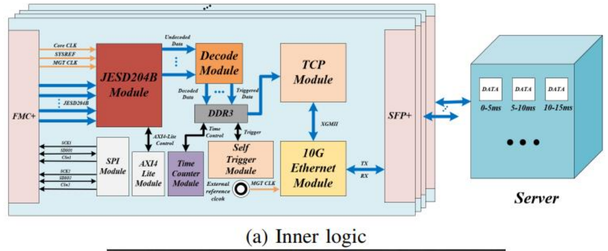
We test ENOB performance of AD9083 chip with several specific frequency sine wave, Fig.2 shows one.



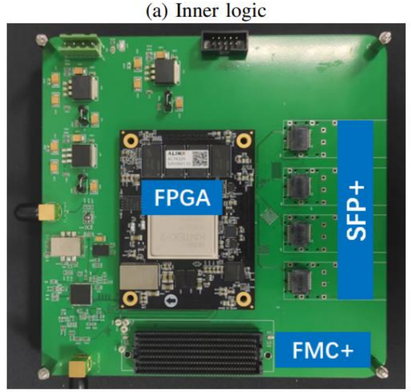
(a) Input requency: 85MHz (b) Distribution of ENOB

Fig. 2: ENOB performance of AD9083

The FPGA receive and process the ADC data real time and then transfer data which has time stamp and head-tail marks now to server. KU040 will be one test borad and XC7K325T will be used later as a substitute. The FPGA inner framework is shown in Fig.3.



(a) Inner logic



(b) FPGA board

Fig. 3: The FPGA part of DAQ

Implementation of multi-board synchronization

Multi-board synchronization includes: 1) front-end synchronization between ADC and FPGA; 2) back-end synchronization between FPGA and server. Fig.4 is the homologous clock source of DAQ system for front-end sync and Fig.5 is the algorithm and principle inner FPGA and server which is for back-end sync.

The realization of digital back-end synchronization mainly depends on time stamps and the head-tail method(HTM). The time information of triggers and channel number will be

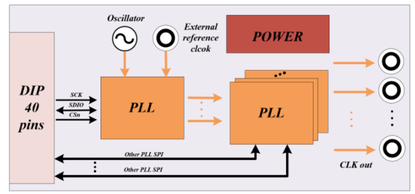


Fig. 4: Homologous clock source of DAQ

added to each data group to clarify the arrival order of data. The data of each channel is packaged, by adding head and tail information, into data packets with a certain size, as shown in Fig.5.

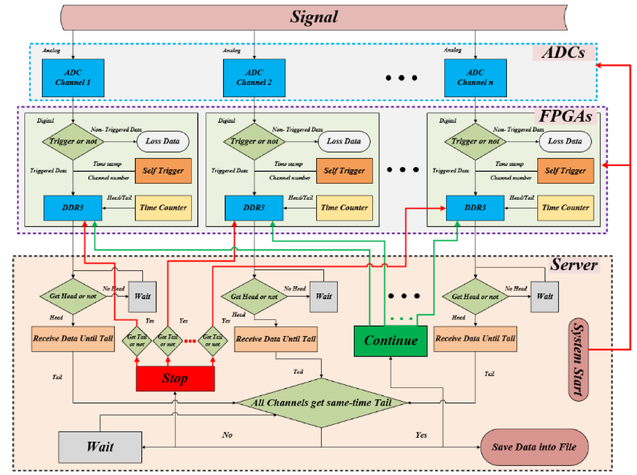
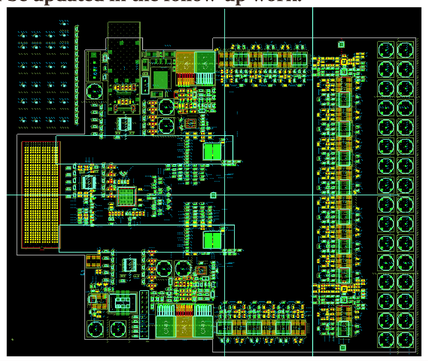


Fig. 5: The back-end synchronization principle

Conclusion

We have successfully designed and tested the performance of AD9083. We are doing the multi-ADC PCB design, as shown in the figure below, and the realization of multi-board synchronization, will be updated in the follow-up work.



YOU CAN ALSO CONTACT

Name: Nan Li

Email: nan.li@mail.sdu.edu.cn

Reference:

[1] J. Pan et al., "Position encoding readout electronics of large area micromegas detectors aiming for cosmic ray muon imaging"
[2] J. Yang et al., "Readout electronics and data acquisition system of PandaX-4t experiment"
[3] C. He et al., "A 500 ms/s waveform digitizer for pandax dark matter experiments"
[4] Q. Wu et al., "Update of the trigger system of the PandaX-II experiment"