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A 4-phase PLL Frequency Multiplier for Wilkinson ADC in SCA ASIC

Waveform digitization is an important research direction in high-energy physics experiments. Compared to the solution based on high speed ADC, switched capacitor array (SCA) has advantages in high sampling rate, low power consumption, and easy multi-channel integration. However, the dead time of SCA is a limitation for many high hit rate applications. In order to reduce the quantization time contributed by the on-chip Wilkinson ADC, a strategy of a high-speed less-bit coarse counter combined with multi-phase clock locking can be adopted. In this case, a high precision PLL with multi-phase is required. This paper presents the design and test of a 4-phase PLL for a 12-bit high-speed Wilkinson ADC employed in our SCA ASIC in research. It contains linear phase and frequency detector (PFD), current steering charge pump (CP), second order loop filter, wideband voltage controlled oscillator (VCO), VCO calibration, locked detector and frequency divider. Moreover, an additional output clock, supporting division by 1, 2, 4, or 8, can be used as a serial readout clock. The PLL has been implemented and fabricated in 0.13 µm CMOS technology, with a core area of is 0.077 mm^2. The test results show that the frequency tuning range of the PLL is achieved from 1 GHz to 2 GHz with a period jitter of 0.9 ps, and the power consumption is 14.5 mW.

Minioral

Yes

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No

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