A 4-phase PLL Frequency Multiplier for Wilkinson ADC in SCA ASIC

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1. Introduction

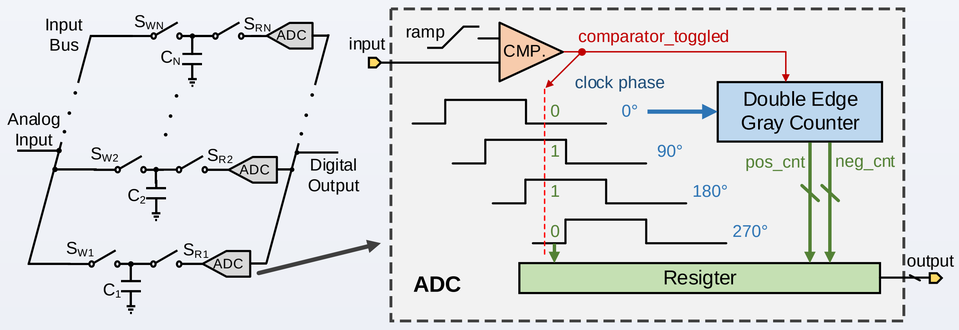


Fig. 1. Architecture of the high-speed ADC in SCA ASIC.

Waveform digitization is an important research direction in high-energy physics experiments. Compared to the solution based on high speed ADC, switched capacitor array (SCA) has advantages in high sampling rate, low power consumption, and easy multi-channel integration. However, the dead time of SCA is a limitation for many high hit rate applications. In order to reduce the quantization time contributed by the on-chip Wilkinson ADC, a strategy of a high-speed less-bit coarse counter combined with multi-phase clock locking can be adopted. In this case, a high precision PLL with multi-phase is required. The architecture of the high-speed ADC in SCA ASIC is shown in Fig. 1. Coarse count value and clock phase information are simultaneously latched when the comparator toggles. According to the phase information of clocks, the count value produced by which clock edge farther from the 'comparator_toggled' signal is used as coarse count to avoid metastability. For example, equivalent 8 GHz quantization speed is achieved by combining 2 GHz clock counting with phase information. Therefore, it is necessary to design a PLL that can work at 2 GHz and has 4-phase output clock. For a low hit rate, the quantization speed can be reduced to save power. Thus, the target frequency range is determined to be 1 ~ 2 GHz. Moreover, an additional adjustable output clock is needed as serial readout clock.

2. Architecture

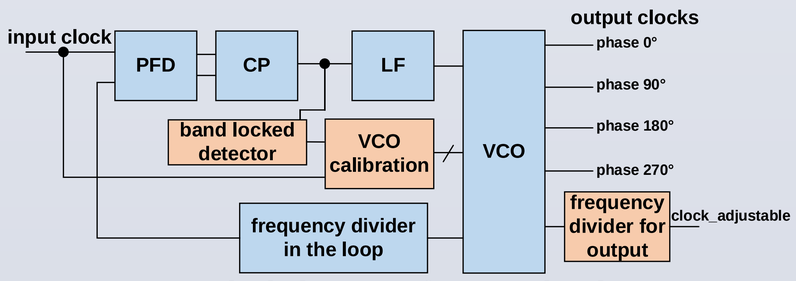


Fig. 2. Block diagram of PLL in this design.

The block diagram of PLL in this design is shown in Fig. 2. It contains phase and frequency detector (PFD), charge pump (CP), loop filter (LF), voltage controlled oscillator (VCO), VCO calibration, band locked detector and frequency divider.

A. VCO

According to the frequency and phase requirement, 2-stage ring VCO is adopted. To achieve the frequency range of 1 GHz ~ 2 GHz, a wideband VCO is used. The schematic of delay cell is shown in Fig. 3. By configuring the 3-bit digital signal 's', the output frequency range can be divided into multiple frequency bands. Control voltage is used for fine adjustment. The variation of frequency of each frequency band with the control voltage is shown in Fig. 4.

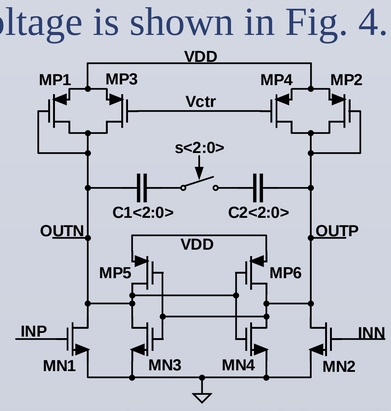


Fig. 3. Schematic of delay cell.

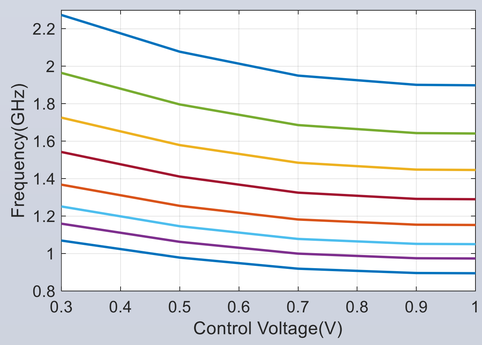


Fig. 4. VCO frequency simulation results.

B. VCO calibration and band locked detector

For the VCO mentioned above, it is important to use the algorithm to select the proper frequency band. The VCO calibration algorithm used is shown in Fig. 5, the signal 's' cycles from 000 to 111 until the PLL locks. The signal 'CAL_DONE' is generated by band locked detector by detecting whether the control voltage is within the design range.

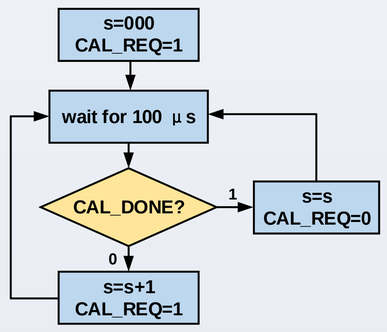


Fig. 5. VCO calibration algorithm.

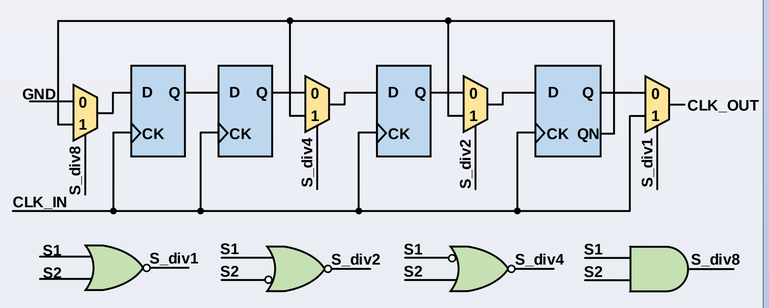


Fig. 6. Schematic of frequency divider for output.

C. Frequency divider for output

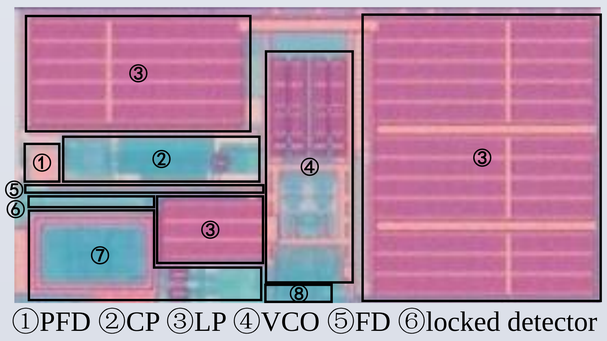
Fig. 6 shows the schematic of the frequency divider for output. By configuring S1 and S2, the divider can be configured to four states: clock buffer, divide-by-2, divide-by-4, and divide-by-8.

D. Other parts

The other parts of PLL , including PFD, CP and LF, were designed based on the classical structures.

3. Performance

A PLL prototype has been designed and fabricated in 130 nm CMOS technology. The area of PLL core is 395 μm × 199 μm. The layout of each circuit is shown in Fig. 7. To evaluate the performance of the PLL, the clock is divided by four and then output outside the chip.



①PFD ②CP ③LP ④VCO ⑤FD ⑥locked detector
⑦VCO Calibration ⑧frequency divider for output

Fig. 7. Micrograph of PLL core.

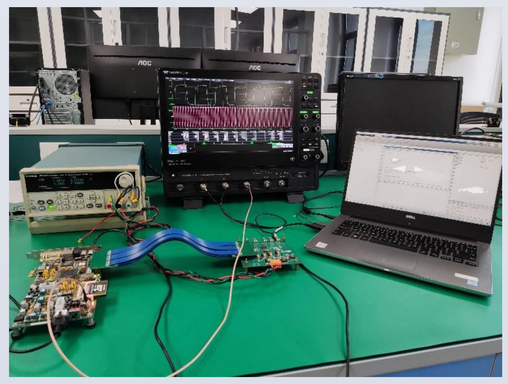


Fig. 8. Photograph of the test bench.

When the output clock frequency is 2 GHz, a period jitter of 0.9 ps is achieved in the time range of 5 ms. When the VCO operates at 2 GHz, the time difference of four clocks can be calculated 134.25 ps, 135.25 ps, 123.25 ps and 107.25 ps. Differential nonlinearity (DNL) contributes error of 50 μV to SCA, which is negligible compared to SCA's noise level. And DNL can be corrected algorithmically.

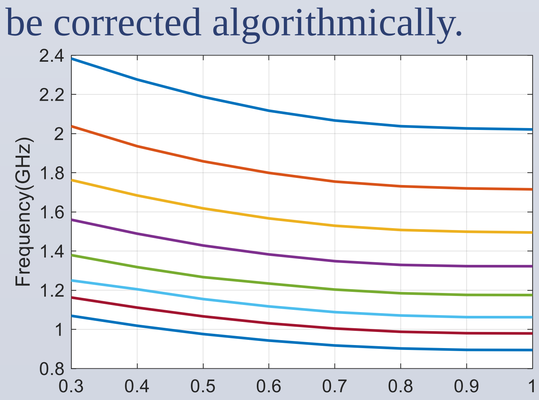


Fig. 9. Frequency coverage test results.

The PLL can be locked at the expected 2 GHz frequency. The frequency of the output clock and its variation with frequency band and control voltage is shown in Fig. 9. The frequency range can cover from 0.89 GHz to 2.38 GHz, achieving the design goal of 1 GHz to 2 GHz. The power consumption of the core part of the PLL is measured 14.5 mW.