



Contribution ID: 27

Type: **Oral Presentation**

PulseDL-II: a system-on-chip neural network accelerator for timing and energy extraction of nuclear detector signals

Thursday 4 August 2022 11:00 (20 minutes)

Front-end electronics equipped with high-speed digitizers are being used and proposed for future nuclear detectors. Recent literature reveals that deep learning models, especially one-dimensional convolutional neural networks, are promising when dealing with digital signals from nuclear detectors. Simulations and experiments demonstrate the satisfactory accuracy and additional benefits of neural networks in this area. However, specific hardware accelerating such models for online operations still needs to be studied. In this work, we introduce PulseDL-II, a system-on-chip (SoC) specially designed for applications of event feature (time, energy, etc.) extraction from pulses with deep learning. Based on the previous version, PulseDL-II incorporates a RISC CPU into the system structure for better functional flexibility and integrity. The neural network accelerator in the SoC adopts a three-level (arithmetic unit, processing element, neural network) hierarchical architecture and facilitates parameter optimization of the digital design. Furthermore, we devise a quantization scheme and associated implementation methods (rescale & bit-shift) for full compatibility with deep learning frameworks (e.g., TensorFlow) within a selected subset of layer types. With the current scheme, the quantization-aware training of neural networks is supported, and network models are automatically transformed into software of RISC CPU by dedicated scripts, with nearly no loss of accuracy. We validate the correct operations of PulseDL-II on field programmable gate arrays and show its improvements compared with the previous version with respect to the performance, power and area. The chip will be taped out with the TSMC 28/65 nm process.

Minioral

Yes

IEEE Member

No

Are you a student?

No

Authors: Dr AI, Pengcheng (Tsinghua University); DENG, Zhi (Tsinghua University); WANG, Yi (Tsinghua University); Mr RAN, Xinchu (Tsinghua University); Mr LANG, Zijian (Tsinghua University)

Presenter: Dr AI, Pengcheng (Tsinghua University)

Session Classification: Architectures, Intelligent Signal Processing & Simulation

