A phototype Readout ASIC for the MTPC detector at CSNS Back-n

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1. Background

The China Spallation Neutron Source (CSNS) is the first pulsed neutron source and the largest scientific facility ever built in China. In order to achieve accurate measurement of neutron nuclear data, it is planned to build a Multi-purpose Time Projection Chambers (MTPC) based nuclear data measurement device in the CSNS back-streaming white neutron source (Back-n).

The proposed MTPC is a cylinder with a diameter of 14 cm, and the readout of the anode signal is done by the 20,000 pad pixels at the bottom of the MTPC. These characteristics limit the size and power consumption of the readout electronics. Moreover, the dead time of the readout electronics is required to be lower than 10 μs to make full use of the high brightness of Back-n and improve the beam utilization efficiency. In addition, the readout electronics should have a wide charge measurement range (from a few fC to 10 pC) due to the large difference in ionization energy loss of some nuclear reaction products.

This demands that the electronics must feature high density, low noise, and low power consumption, and thus it is necessary to employ a suitable ASIC (Applications Specific Integrated Circuit) to satisfy these requirements. The detailed requirements for the ASIC are listed in Table 1.

Table. 1. Requirements for the electronics.

Parameter	Value
Total readout channels	20,000
Dynamic Range	2 pC & 10 pC adjustable
Equivalent noise charge (ENC) @ 100 pF Cin @ Peaking time = 1 μs	< 1 fC RMS @ 2 pC < 5 fC RMS @ 10 pC
Integral Non-Linearity (INL) @ Peaking time = 1 μs	< 2%
Dead time	< 10.3 μs
Output Swing	~ 1 Vpp, differential
Power consumption	< 10 mW/channel

2. ASIC ARCHITECTURE

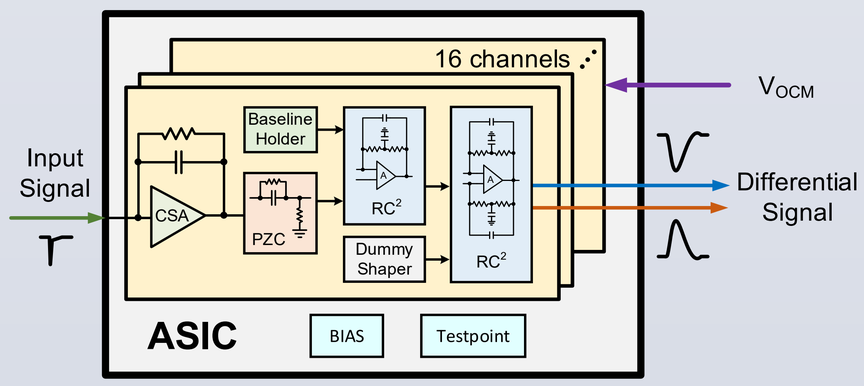


Fig. 1. Block diagram of the prototype ASIC.

A simplified block diagram of the prototype ASIC is shown in Fig. 1. In the first version prototype ASIC, we have integrated the analog signal manipulation of 16 channels within one chip. Each channel comprises a Charge Sensitive Amplifier (CSA), a pole-zero cancellation (PZC), two bridged-T filters, a baseline holder (BLH), and a fully differential output buffer. The PZC and two bridged-T filters jointly form a CR-$(RC)^4$ Semi-Gaussian shaper.

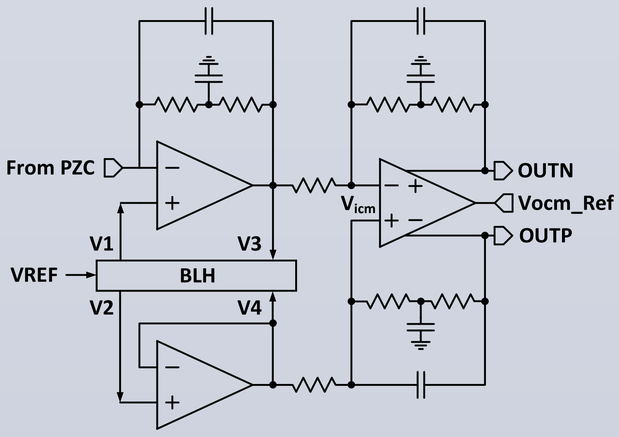
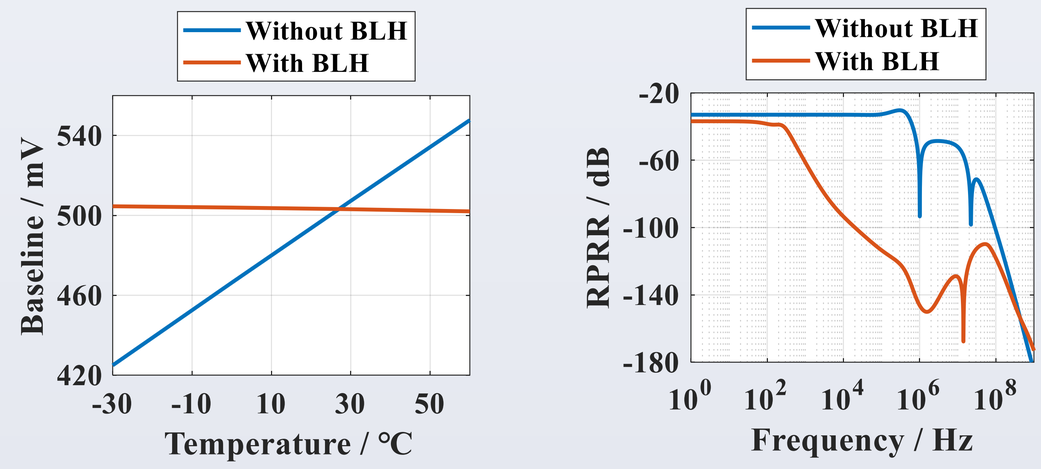


Fig. 2. Schematic diagram of the shaper network.

In this prototype ASIC, the structure of the differential filter network as shown in Fig. 2 is proposed. It is implemented with two bridged-T filters and a BLH circuit. The power consumption of the BLH circuit is only 20 μW, but it can reduce the influence of temperature drift and process corner on the output baseline. Besides, it can reduce the potential noise or crosstalk from the reference path.

To confirm the performance of the BLH circuit, a series of simulations have been conducted. The temperature analysis of Fig. 3(a) approves that the differential output baseline with the BLH circuit has better stability in the temperature range of -30 ℃ to +60 ℃. As for the Reference Rath Rejection Ratio (RPRR), the simulation result is shown in Fig. 3(b) which indicates that the RPRR with the BLH circuit is at least 50 dB better than that without BLH circuit over the major frequency component of the output signal from 100 kHz to 10 MHz.



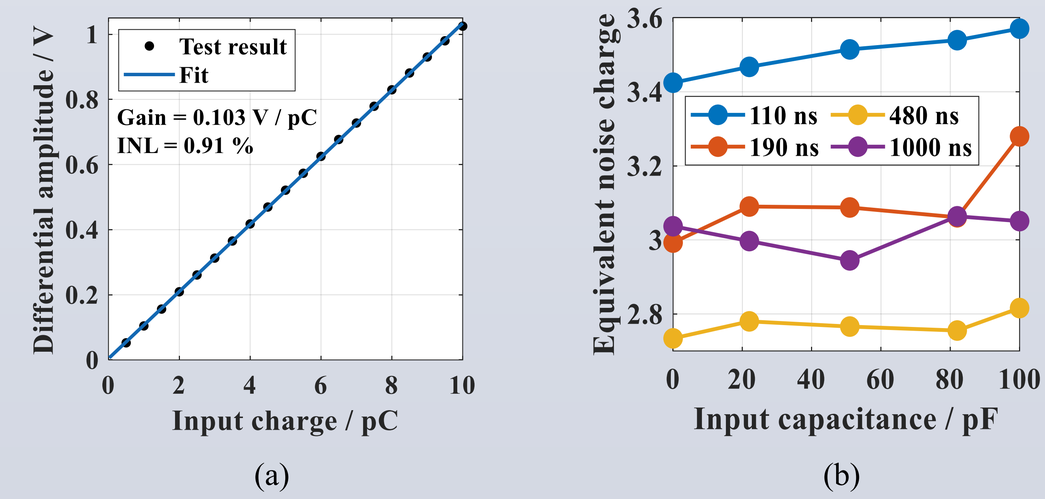
(a) (b)

Fig. 3. (a) Simulation result of the output baseline stability, (b) Simulation result of the Reference Rath Rejection Ratio (RPRR).

3. TEST RESULTS

After fabrication of the ASIC, we set up a test platform in the laboratory and conducted a series of tests. By sending signals with different charge into the chip, we can measure the gain and linearity. Fig. 4(a) shows the fitting result of the differential amplitude versus the injected charge. The conversion gain is 0.103 V/pC and the maximum INL is 0.91%, which is well below the design requirement.

The noise of the ASIC is measured by using the oscilloscope. The output is continuously sampled, and 5,000,000 samples are used to calculate the variance. The measurement results of ENC for different peaking time and input capacitance are shown in Fig. 4(b). According to the test results, the ENC is better than 3.6 fC for all peaking time at 10 pC dynamic range. Therefore, the noise performance satisfies the requirements.



(a) (b)

Fig. 4. Test results at 10 pC dynamic range. (a) Fitting result of Gain and INL, (b) ENC versus peaking time and input capacitance.

4. SUMMARY

In conclusion, A new prototype ASIC has been designed to read the MTPC detector at CSNS Back-n White Neutron Source. The chip integrates 16 channels and provides eight possible combinations of conversion gain and peaking time. It has been tested and the power consumption is only 8.61 mW per channel. In the test condition of 100 pF input capacitance, the ENC maintains to be lower than 3.1 fC at 10 pC dynamic range. The maximum INL equals 0.91% and the dead time is no more than 5 μs. Besides, this ASIC has a low ambient temperature dependency. The test result indicates that this prototype ASIC fully satisfies the design requirements.