

23rd Virtual IEEE Real Time Conference Abstract ID #19

Author: Lin Jiang, Tianhao Wang, Jingjun Wen, Tao Xue

Motivation

CDEX project which aims at search of Dark Matter, will soon come to CDEX-100 period in about 2 years. CDEX-100 consists of 100 HPGe (high-purity germanium) array detectors weighing about 1kg, each detector has a high gain channel, so there are 100 channels in total. Taking the output RMS noise of C1B as a reference, which is 30eV, the relationship between the data bandwidth and energy threshold of the direct detection of CDEX-100 dark matter is as follows,

Table. Energy Threshold v.s. Data Bandwidth.

$\sigma = 30 \text{ eV}$	Threshold (eV)	Noise Trigger Rate(cps)	Single Channel 125 MSPS / 16-bit 120us Record Length per Event		CDEX-100 100 low energy detection channels 125 MSPS / 16-bit 120us Record Length per Event	
			Readout Bandwidth(GB/s)	Data Generated(TB/day)	Readout Bandwidth(GB/s)	Data Generated(TB/day)
	160	6.026	0.000175	0.0142	0.0175	1.48
	120	6775.259	0.2033	15.9656	20.33	1596.56
	100(Triggerless transfer)		0.25	20.5994	25	2109.38

System Design and Signal Integrity Testing

This work has preliminary designed an readout system (Readout over PCIe, RoPe) for CDEX-100. The whole system is built on Xilinx Zynq 7Z100 SoC and support 80Gbps of input bandwidth based on 2 QSFP+ optical link and 40Gbps theoretical output bandwidth based on PCIe Gen2 x8 link.

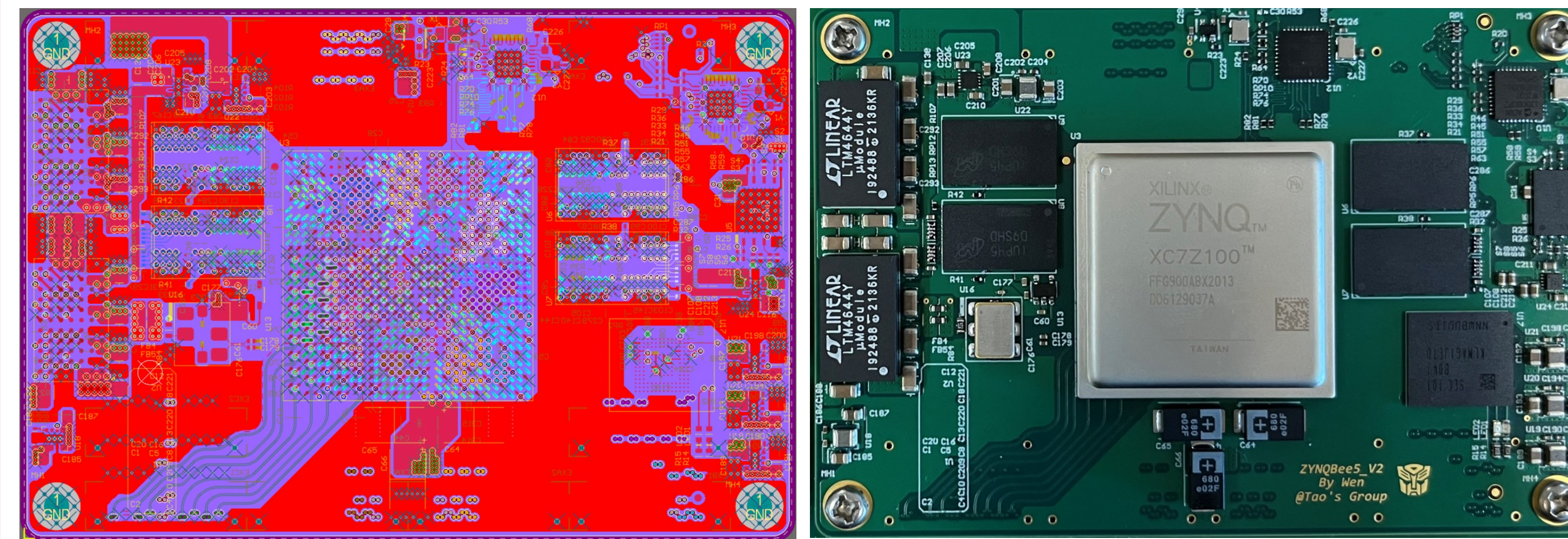


Fig. Core readout module based on Xilinx ZYNQ XC7Z100 SoC.

Data Transfer Test Result

Based on several factors influencing PCIe performance, this paper calculates the transmission environment and theoretical transmission bandwidth faced by RoPe. The measured maximum transmission bandwidth can reach 3.55GB/s, which is consistent with the calculated results 3.6GB/s. The performance law of software speed test is basically the same as that of hardware speed test. When the data packet reaches a certain volume, the software speed will be close to the hardware speed, which can reach more than 3.5 GB/s.

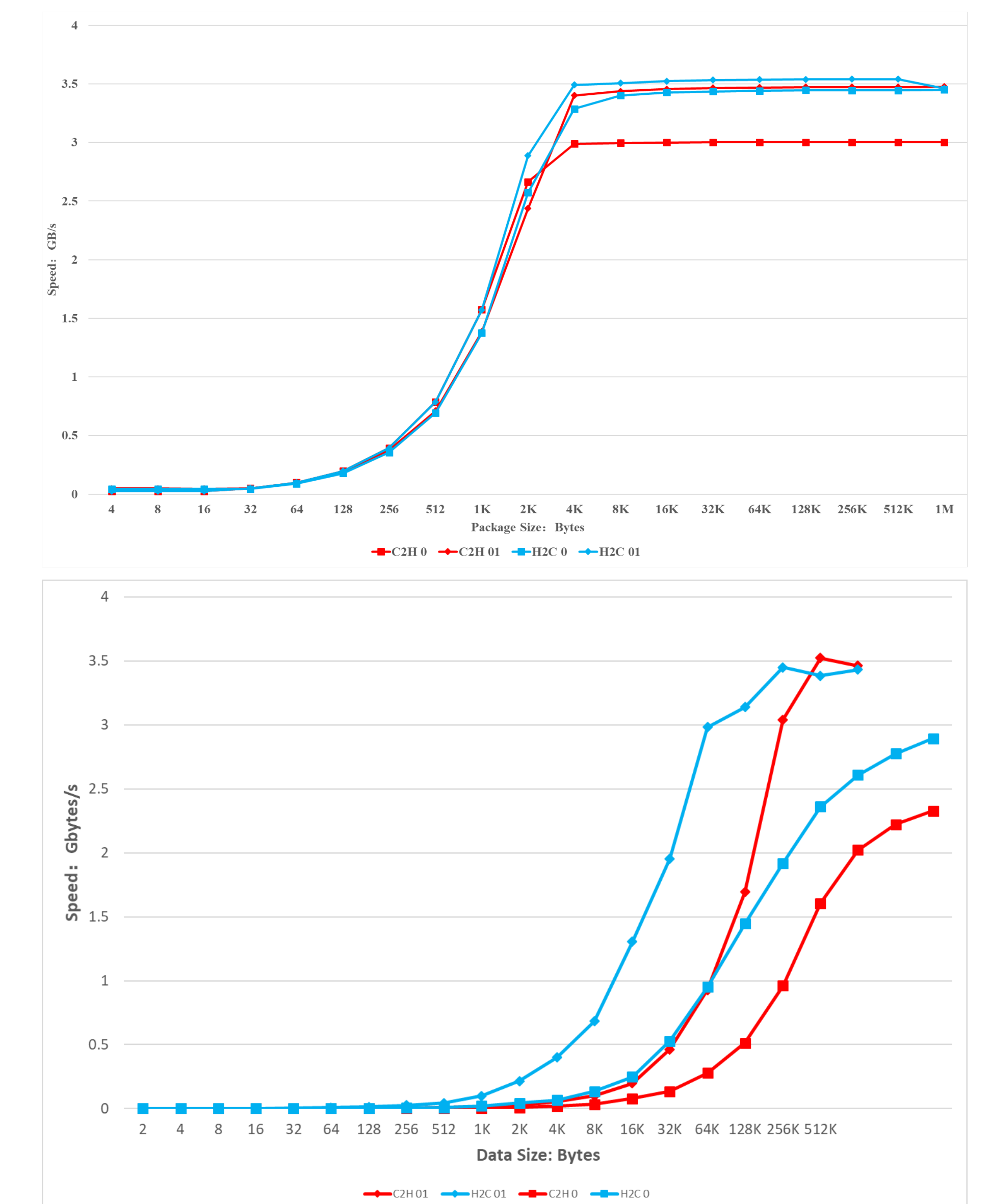


Fig. RoPe V1.0 Bidirectional Single and Dual Channel Hardware (Top) and Software (Bottom) Speed Measurement Results (MPS = 256 Bytes, MRRS is 512 Bytes).

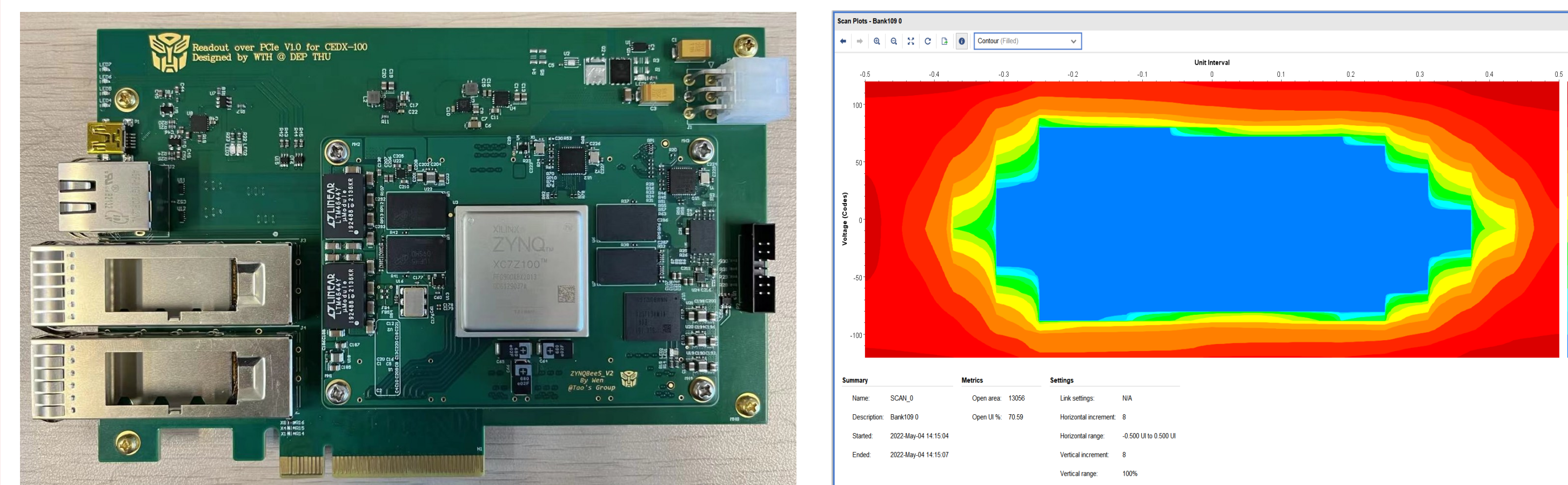


Fig. Physical photo of RoPe (left) and IBERT test interface (right).

PCIe Gen2 x8 interface with KY-PCIE-LPBK test version to achieve self-loopback for signal integrity testing, the 5Gbps signal eye opening ratio of 8 links is greater than 70%. Meanwhile, the QSFP+ interface is connected through a self-loopback module for the same test, the 10Gbps signal eye opening ratio of 8 links is greater than 44%.

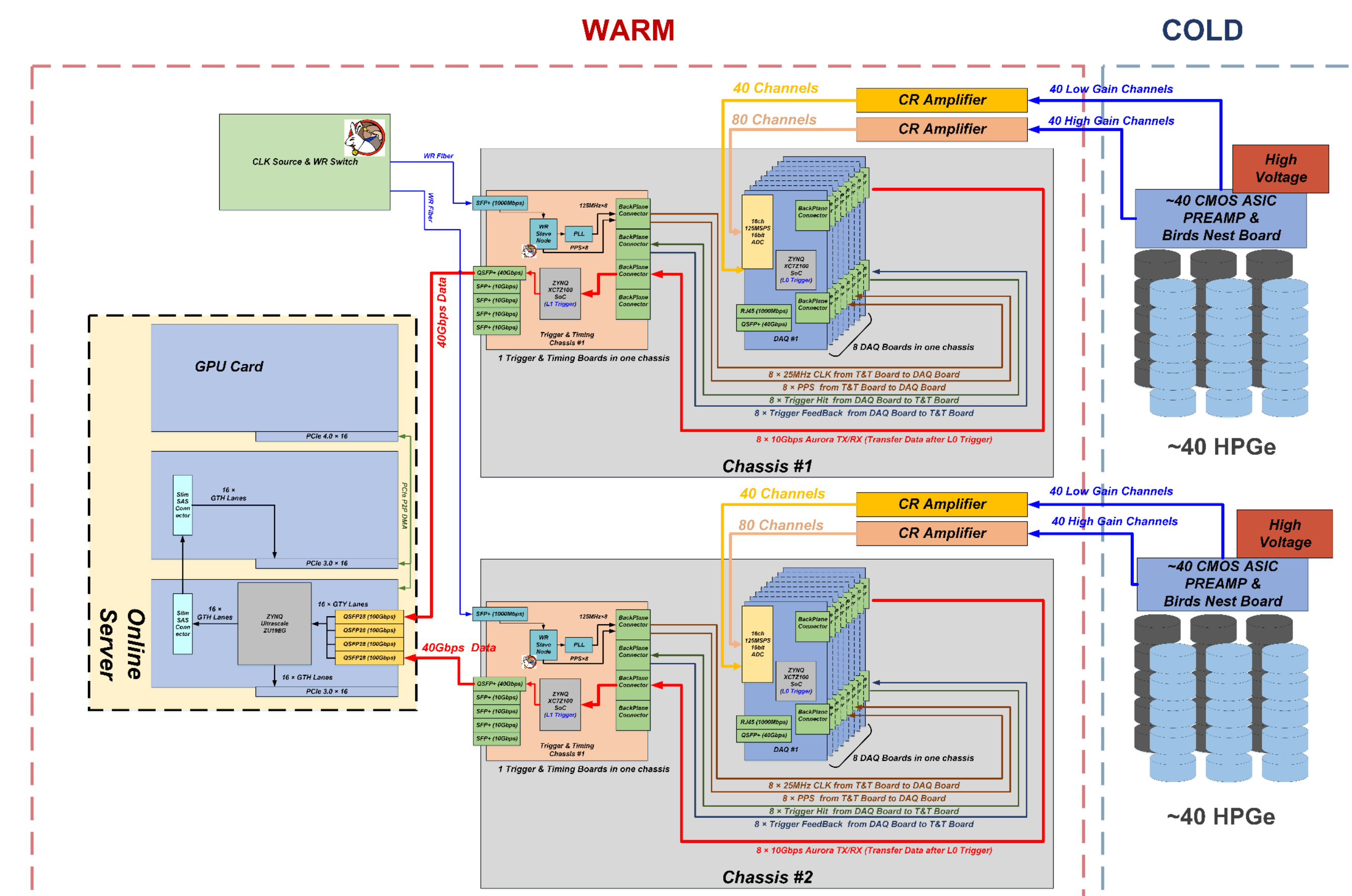


Fig. CDEX-100 Readout System Architecture.