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## A Low power 4 × 14-Gbps VCSEL Driver in 65 nm CMOS for Particle Physics Experiments

This paper presents the novel design and the test results of a 4×14-Gbps Vertical-Cavity Surface-Emitting Laser (VCSEL) driver ASIC fabricated in a 65 nm CMOS process for particle physics experiments. The driver ASIC includes four independent channels and a I2C module. Each channel consists of a limiting amplifier stage, a novel output driver stage and bias circuits. The limiting amplifier stage is composed of an equalizer and two pre-drivers. The equalizer adopts continuous time linear equalizer (CTLE) structure with inductance peaking to compensate for high-frequency attenuation caused by parasitic form PCB transmission line and input PADs. And the pre-driver uses shared inductor structure to expand the bandwidth. The output driver stage converts the voltage signal output by limiting amplifier stage into high-speed current signal, and modulates VCSEL coordinating with bias circuit. The proposed output driver stage provides an effective way to contribute current to the VCSEL. A CTLE pre-emphasis structure and the feedforward capacitor compensation technology are employed in this output driver stage to increase the bandwidth.

The 4×14-Gbps VCSEL driver ASIC has been taped out in 55 nm CMOS technology and tested successfully. The dimension of chip is 2000 μm×1230 μm, and the power consumption is 44 mW/ch at 14-Gbps with 1.2V power supply. Wide-open 14-Gbps optical eye diagram has been captured by oscilloscope and the eye passed the eye mask of the 10-Gbps fiber channel standard. The measured peak-to-peak jitter is 15.8 ps with RMS jitter is 3.02 ps.

### Minioral

Yes

### IEEE Member

No

### Are you a student?

Yes

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