Readout electronics for the CEE Zero Degree Calorimeter at HIRFL
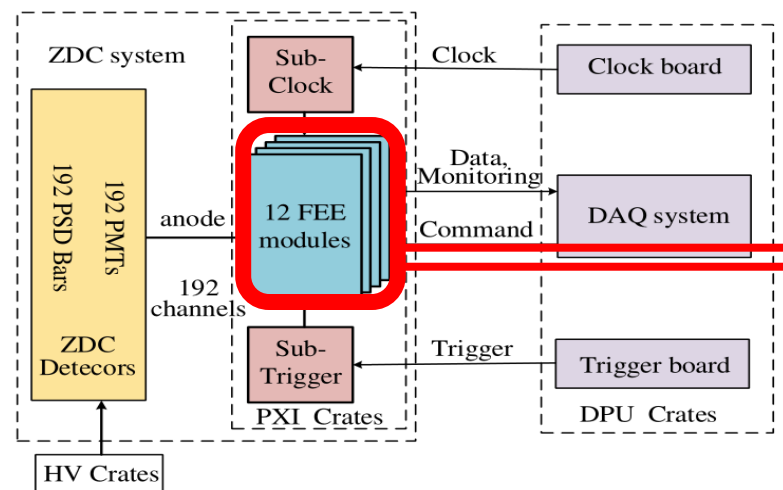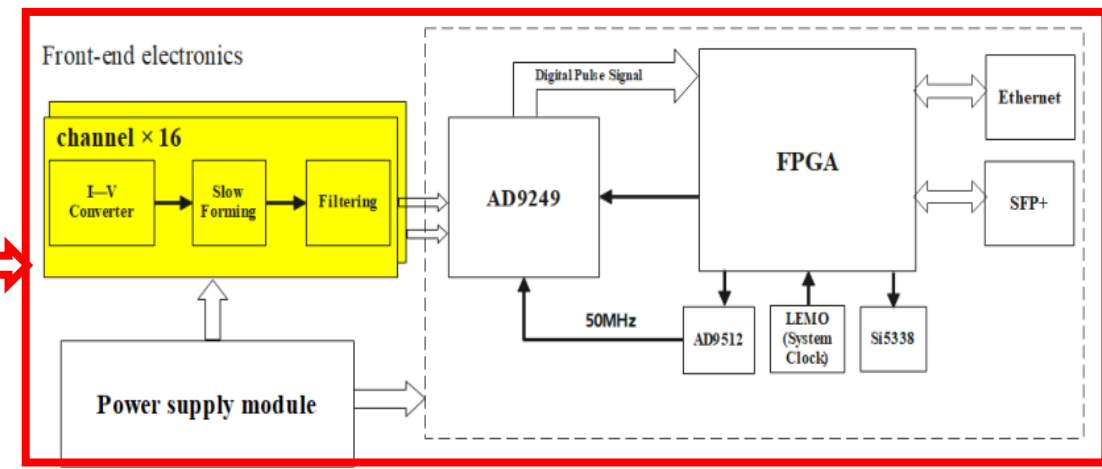

Architecture of the readout electronics for ZDC.

Architecture of the FEE.

The readout electronics consists of 12 FEE modules, one FEE has 16 channels. The FEE, sub-trigger board, and sub-clock board are inserted in the same 6U standard PXI.

Each FEE channel mainly includes the same I-V conversion, slow shaping, and filtering circuits. Each channel converts the filtered voltage pulse signal into a digital signal and sends it to the FPGA for baseline recovery, digital filtering, peak picking, and other digital signal processing.