Readout electronics for the Zero Degree Calorimeter at HIRFL-CEE experiment

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Abstract: **This paper presents the readout electronics of the Zero Degree Calorimeter at the HIRFL CEE experiment. The readout electronics consists of 12 FEE (Front End Electronics) modules, the sub-trigger module, the sub-clock module, and one HV (High Voltage) crate. The test results indicate that the noise performance is less than 0.4 mV (RMS), the nonlinearity of the full readout electronics is less than 0.06%, and the inconsistency among channels is less than 2.5%. In addition, cosmic ray and beam test results demonstrate that the readout electronics perform well.**

Introduction

The CSR External-target Experiment (CEE) at the Heavy Ion Research Facility at Lanzhou (HIRFL) will be the first large-scale experiment in nuclear physics independently developed in China, covering the GeV energy regime. As a major detector, the Zero Degree Calorimeter (ZDC) measures the centrality and reaction plane of the nuclear-nuclear collision from the hadron background.

The readout electronics of the CEE - ZDC contain channels to read all the Plastic Scintillator bars. It can work at the event rate of up to 20 kHz. Besides, the readout electronics communicate with the global trigger system, the global clock system, and the global DAQ system of the CEE experiment. E DAQ system to operate correctly in the CEE experiment.

The readout electronics for ZDC.

Fig. 1 shows the overview architecture of the readout electronics of the ZDC detector. The readout electronics consists of 12 FEE modules, each of which has 16 channels. In addition, one HV (High Voltage) crate provides a high voltage supply to the PMTs. The FEEs receive the negative charge pulse signal from the PMT anode, perform I-V conversion on the charge, and digitize them under the self-trigger signal's control. Then, the FEEs use on-board FPGA to select the valid events data upon the trigger signal from the global trigger system, package the data, and transmit it to the DAQ system.

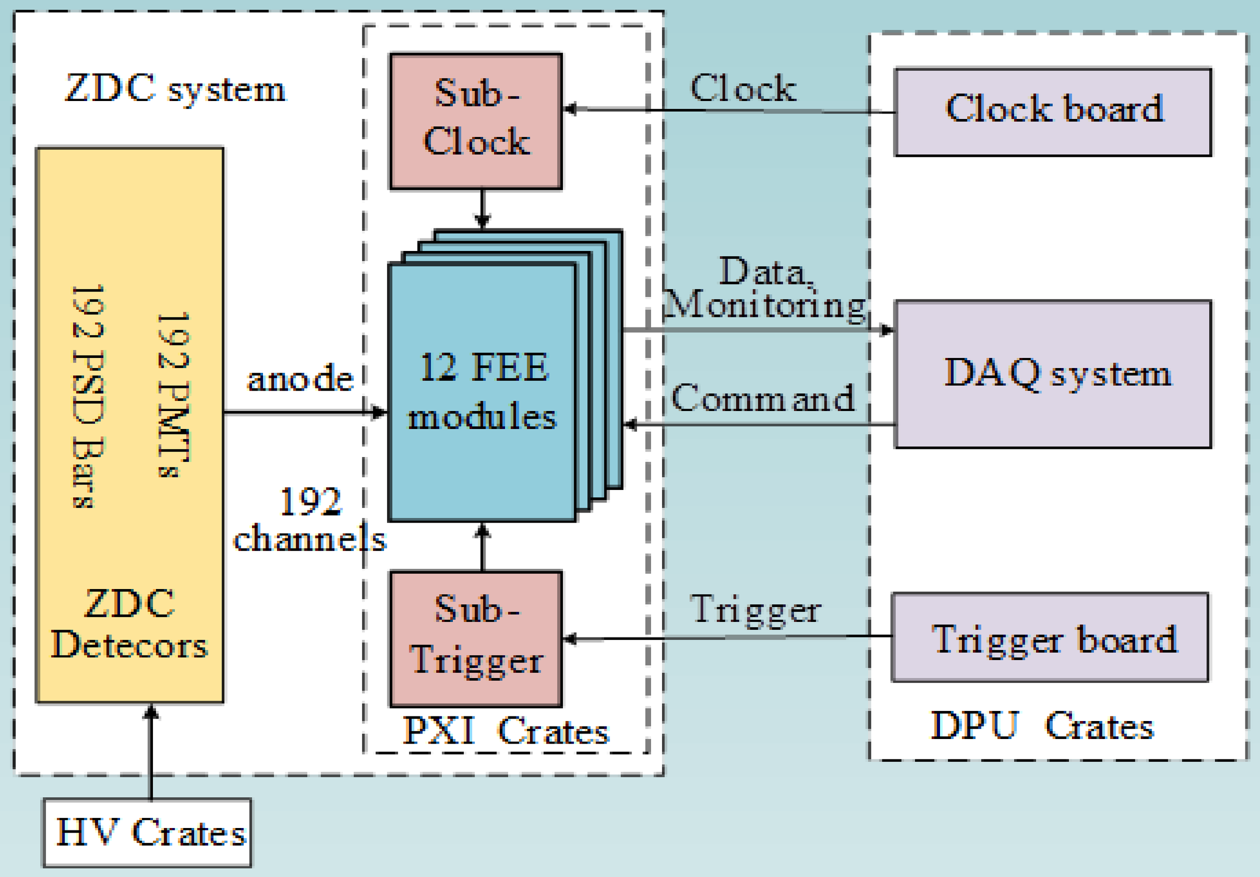
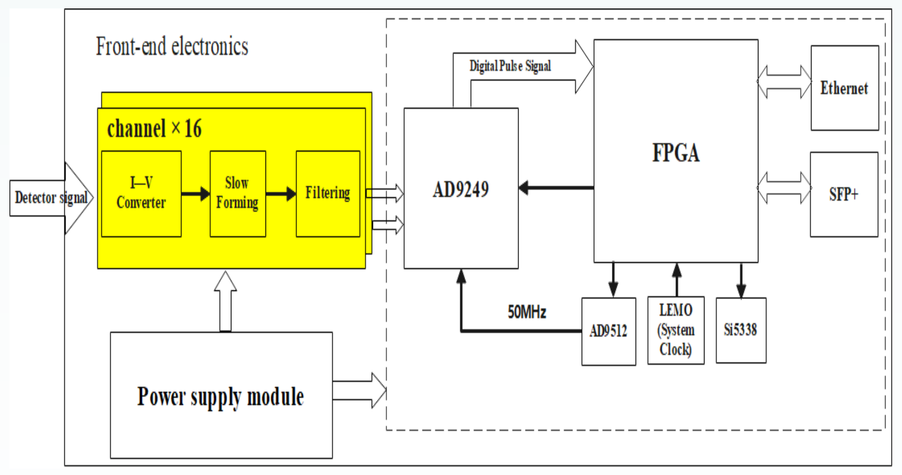


Fig. 1. Architecture of the readout electronics for ZDC.

A. Hardware design of the FEE

Fig. 2 shows the FEE design overview and the FEE's physical photo, respectively. Each FEE channel mainly includes the circuits for I-V conversion, slow shaping, and analog filtering. Each channel converts the filtered voltage pulse signal into a digital signal by the onboard 16-channel 14-bit ADC (AD9249) at a sampling rate of 50 MHz and sends it to the FPGA for baseline recovery, digital filtering, peak picking, and other digital signal processing. An optical fiber link sends the ex-post data to the DAQ system. In addition, the Ethernet interface is used for onboard debugging.



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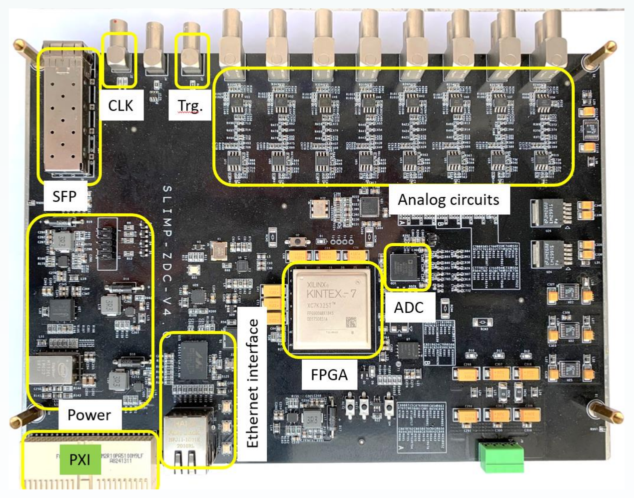


(b)

Fig. 2. a. The overview of the FEE design. b. The physical photo of the FEE.

B. FPGA logic design of the FEE

The FEE FPGA design mainly contains four parts: digital signal processing, command configuration, data transfer, and clock configuration.

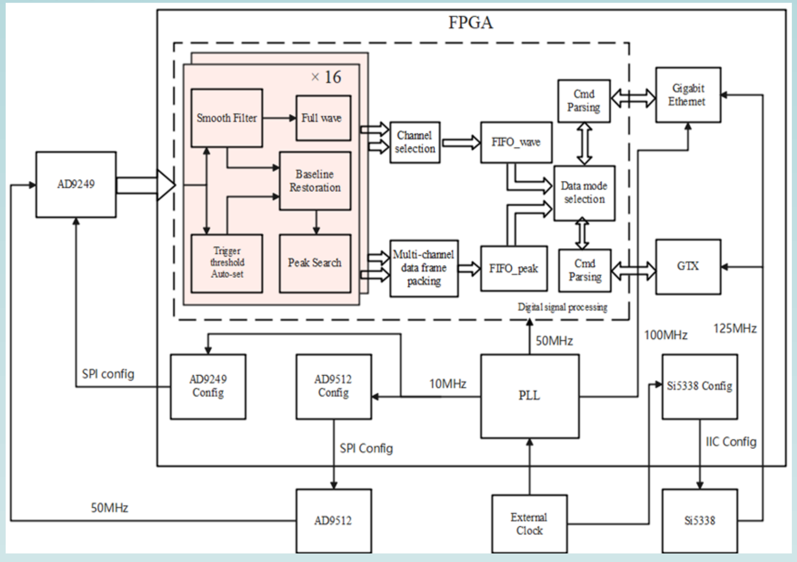
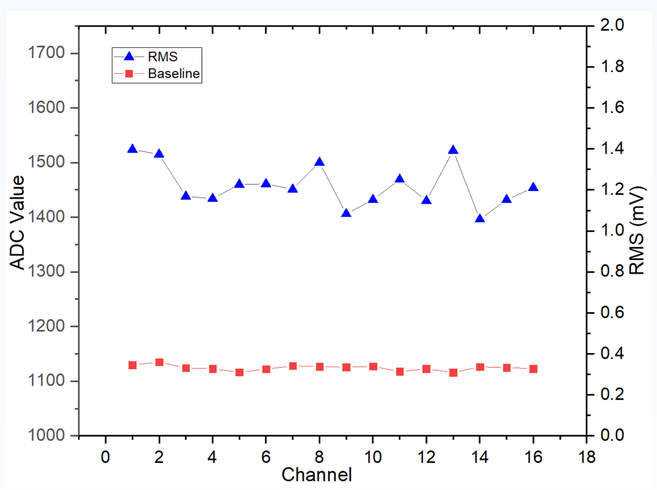


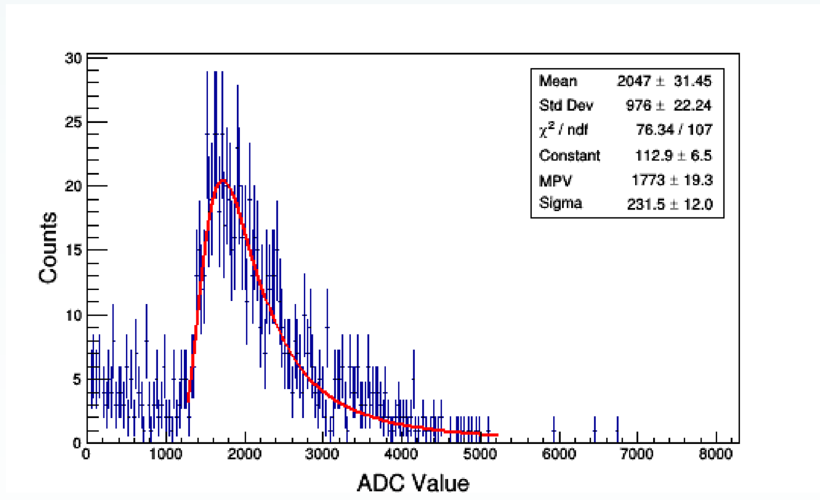
Fig. 3. The diagram of the FPGA design.

Performance measurement

Fig.4.a. shows the ADC output and the RMS for the 16 channels on one FEE. The test results indicate that the noise performance is less than 0.4 mV (RMS), the non-linearity of the full readout electronics is less than 0.4%, and the channel consistency is better than 2.5% receptively. In addition, cosmic ray and beam test results demonstrate that the readout system can perform well. Fig.4.b. is the Landau distribution fitting of the cosmic ray energy spectrum, and the fitted peak is around 1773 ADC value. The test results show the readout electronics satisfy the physics requirements.



(a)



(b)

Fig. 4. a. Baseline and Noise of one FEE. b. Landau distribution fit of cosmic ray spectrum.