Characterization of a 16-Channel LArASIC for the Front-end Read-out Electronics System at DUNE Experiment

Eaglekumar G. Tarpara
On behalf of the DUNE collaboration

Brookhaven National Laboratory, NY, USA

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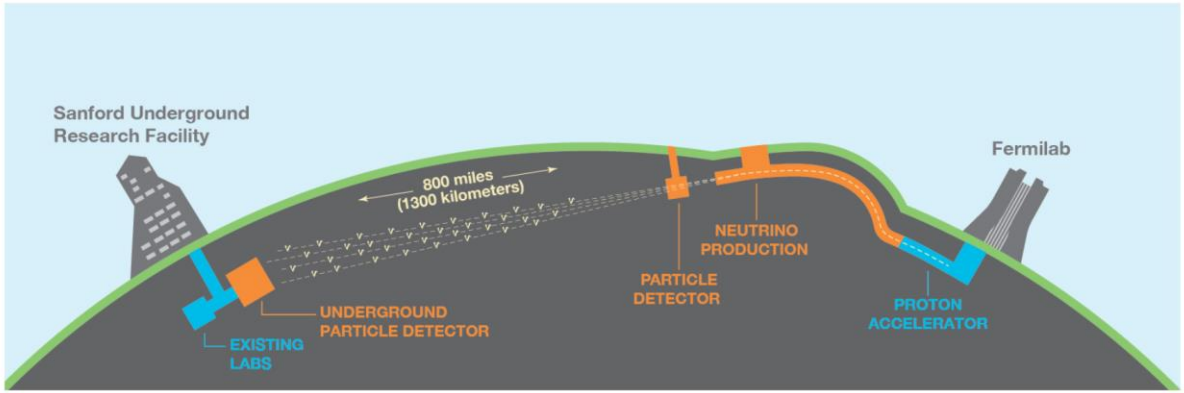
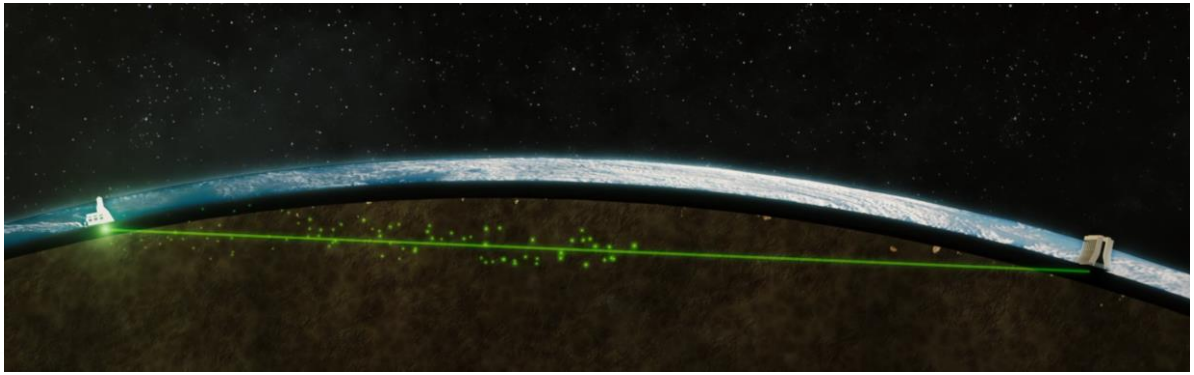
Long Baseline Neutrino Program: LBNF/DUNE



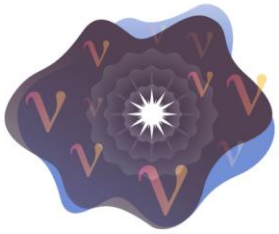
DUNE Science Colllaboration

- ~1400 Collaborators
- ~200 Instittuites
- ~30 Contries + CERN



Primary science goals

Neutrino/antineutrino oscillations – Search for the origin of matter



Supernova Neutrino Bursts – Learn about neutron stars and black holes

Proton decay - shed light on the unification of nature's forces

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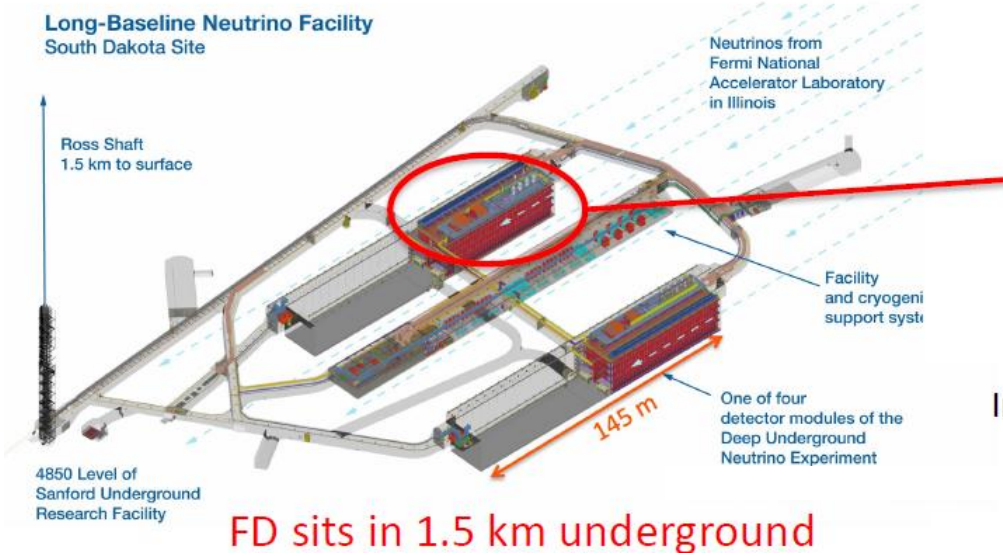
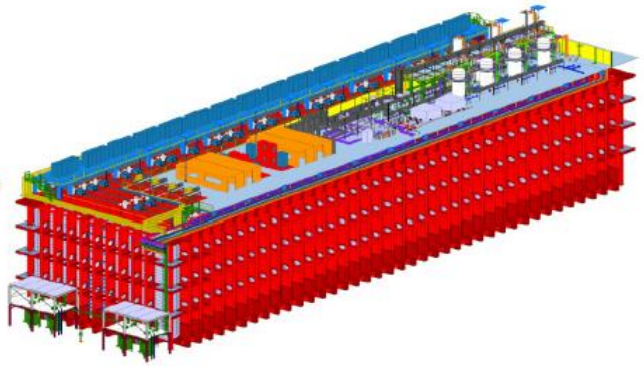
Single-Phase LArTPC for the DUNE Far Detector Modules



FD sits in 1.5 km underground

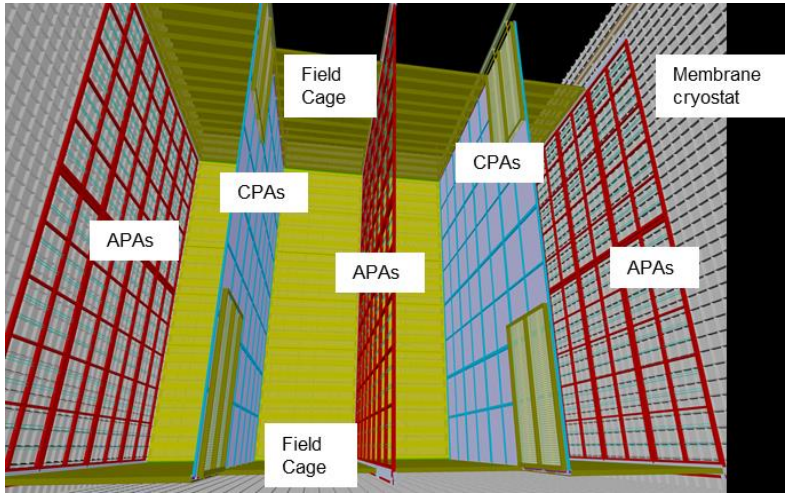


Outer:
65.8 m (L)
18.9 m (W)
17.8 m (H)

Inner active volume: 14.0 m (W)×12.0 m (H) × 58.2 m (L)

DUNE first 17 kt Far Detector LArTPC CE

- 150 APA units
- 384,000 channels
- 24,000 FE ASICs/24,000 ADC ASICs
- 6,000 COLDATA ASICs
- 3,000 Front End Mother Board assemblies
- Aim for 30 years of operation without replacement and maintenance



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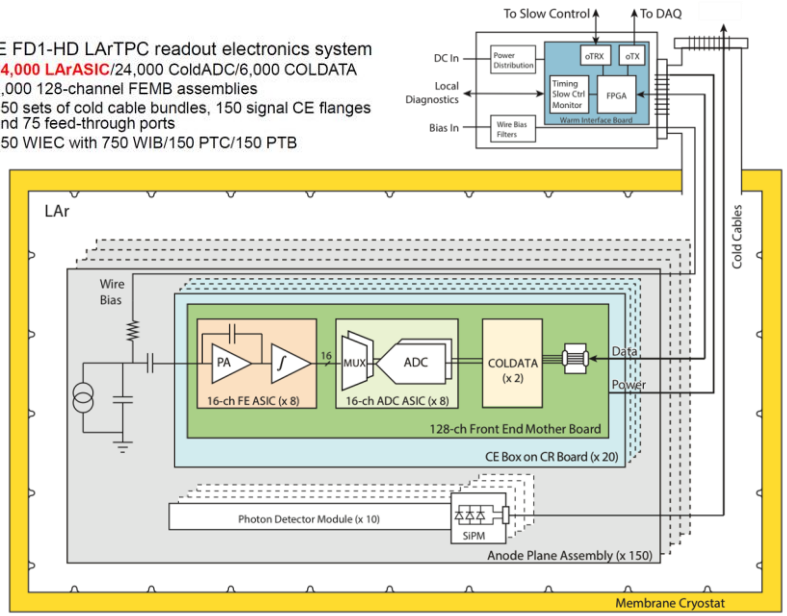
LArTPC CE

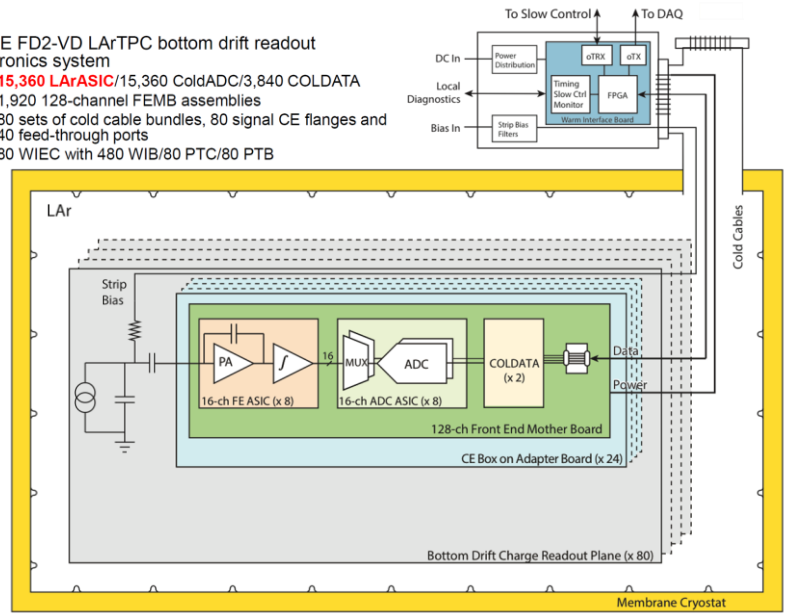
FD1-HD

- DUNE FD1-HD LArTPC readout electronics system
  - 24,000 LArASIC/24,000 ColdADC/6,000 COLDATA
  - 3,000 128-channel FEMB assemblies
  - 150 sets of cold cable bundles, 150 signal CE flanges and 75 feed-through ports
  - 150 WIEC with 750 WIB/150 PTC/150 PTB



FD2-VD

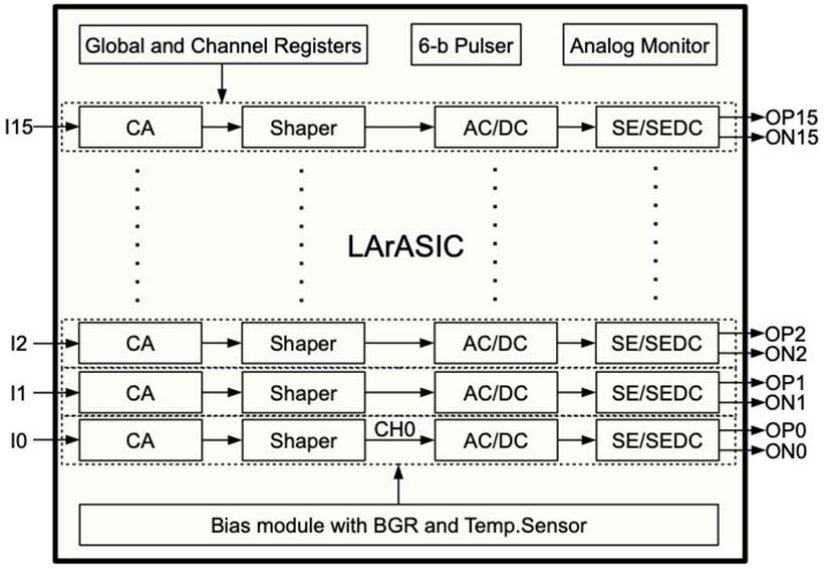
DUNE FD2-VD LArTPC bottom drift readout electronics system
- 15,360 LArASIC/15,360 ColdADC/3,840 COLDATA
- 1,920 128-channel FEMB assemblies
- 80 sets of cold cable bundles, 80 signal CE flanges and 40 feed-through ports
- 80 WIEC with 480 WIB/80 PTC/80 PTB

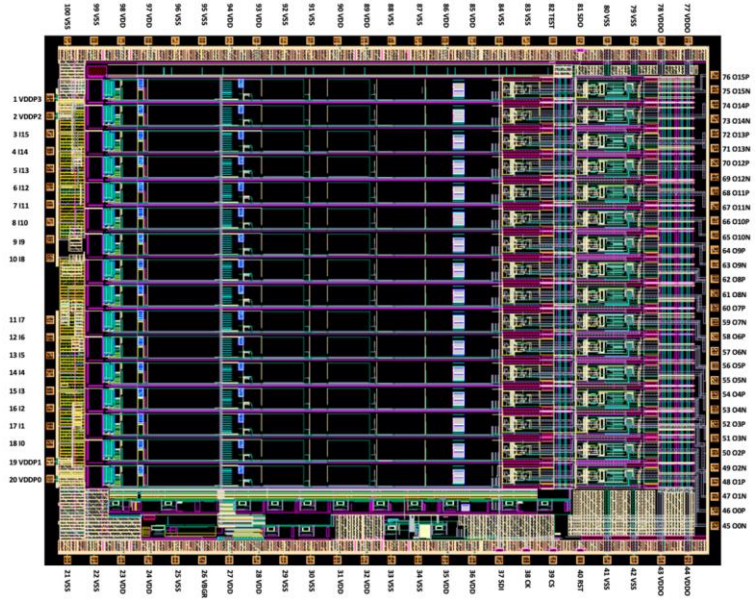


ProtoDUNE-II

- The plan is to install and operate the FD1-HD and FD2-VD production components in ProtoDUNE-II during 2022/2023.
- This will be used to validate both the detector components and the processes put in place to construct and install them
- ProtoDUNE-II HD
  - 4 APAs (2560 CH/APA)
    - Two upper DUNE APAs - CE will be installed at top
    - Two lower DUNE APAs - CE will be installed at bottom
  - 20 Xilinx Zynq+ WIBs
  - 4 WIECs
- 80 FEMBs (CE boxes) for ProtoDUNE-II HD
  - 640 LArASIC + 640 ColdADC + 160 ColdDATA chips
- 48 FEMBs (CE boxes) for ProtoDUNE-II VD
  - 384 LArASIC + 384 ColdADC + 96 ColdDATA chips

LArASIC P5B





Technology	180 nm CMOS – 1-poly, 6-metal, MiM cap, sil blk resistors			
Supply Voltage	1.8 V			
Temperature Range	77 – 300 K (-196 – 27 °C) optimized for 87k (-186 °C)			
Number of Channels	16			
Max Single-Ended Output Swing	1.4 V peak to peak (0.2 – 1.6 V)			
Gain Selection (mV/fC)	4.7	7.8	14	25
Full-Scale Input Charge (fC)	300	180	100	56
Baseline selection	200 mV (collection mode)		900 mV (induction mode)	
Charge Preamplifier Polarity	Negative (collection mode)		Bipolar (induction mode)	
Adaptive-Reset Current Selection (nA)	0.1	0.5	1	5
Shaper Peaking Time Selection (µs)	0.5	1	2	3
Output Coupling	AC (100 µs HPF time-constant)		DC	
Output Selection	Shaper	SE buffer	SEDC buffer	
Total Channel Settings	1024			
Integrated Test Capacitor	200 fF			
Temperature Sensor	0.8728 V @ 25°C + 2.868 mV/°C			
Integrated Pulse Generator	6-bit DAC based			
Configuration Control	SPI interface with 144 register bits			

- Goal of P5B LArASIC
  - Remove RQI subtraction to fix a few non-operational channels in LN2 (Success)
  - Modify SEDC buffer for stable and low noise operation (Success)
  - Modify Test Charge Injection Pulser DAC in terms of its linearity (Success)
  - Retain improvements achieved in P4 (ledge effect elimination, bandgap cold startup) (Success)
  - Apply Enhance ESD protection scheme to tolerate higher discharge (Success)

LArASIC QC

- LArASIC is designed to operate in liquid Argon (87K)
  - Appropriate design rules for operation in cryogenic liquids are used to ensure LArASIC will operate with minimal losses of channels throughout the expected lifetime of the DUNE experiment (~30 years)
  - FEMBs in a cryostat (liquid Argon) is not accessible for repair or replacement
- We will be using around 1024, 24000 and 15360 LArASIC (P5B version) packaged chips for ProtoDUNE-II, DUNE FD1-HD and DUNE FD2-VD experiments, respectively.
- The systematic characterization and performance testing of the LArASIC chip at cryogenic temperature is vital for the quality and reliability of detectors at ProtoDUNE-II and DUNE experiments.
- The TPC electronics consortium plan involves having multiple sites using the same QC procedure.
- The plan assumes each chip passing the warm test will be tested at LN2 to assure the cold yield

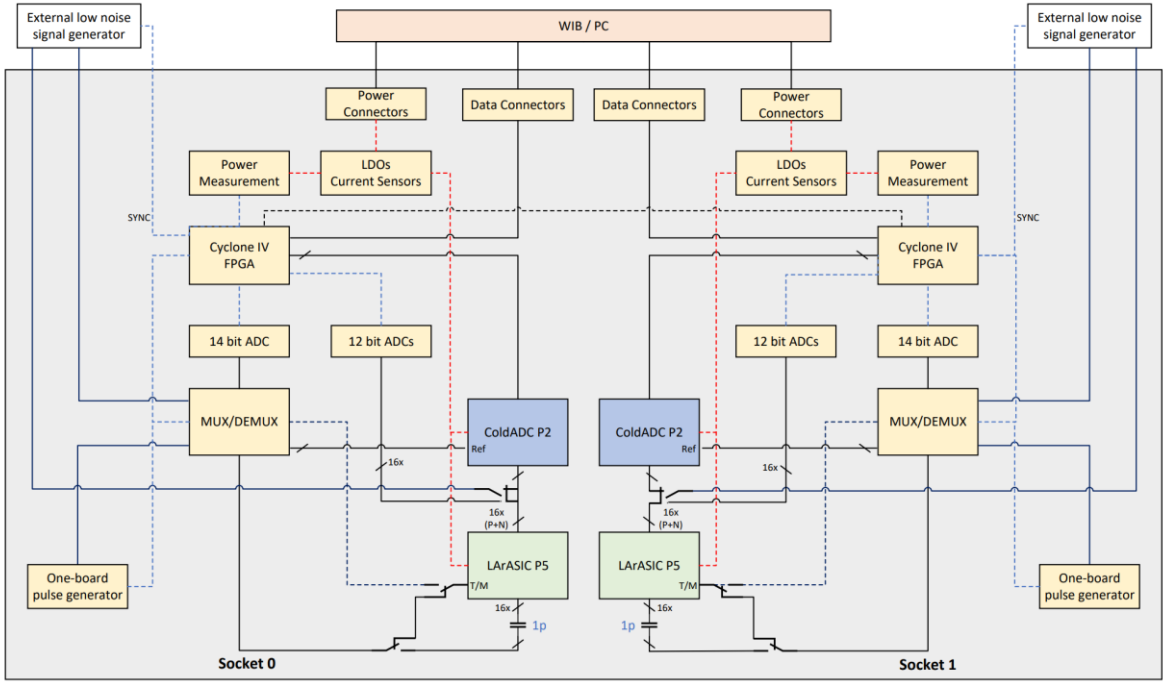
LArASIC QC Items Recommendation

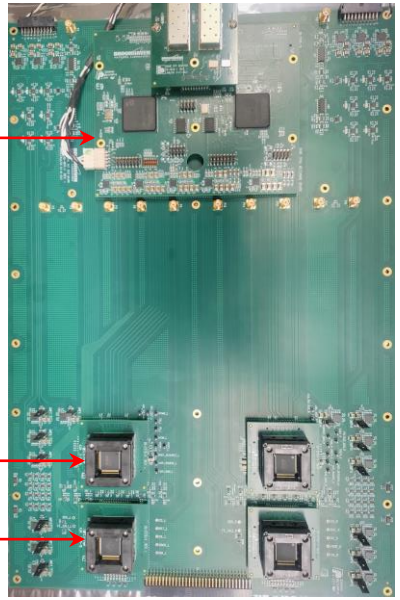
Items	Description
Power consumption	Each LArASIC has 3 power rails (VDDP, VDDA, VDDO) of which voltage and current are recorded under 3 configurations (default, SE on, and SEDC on)
Power cycle	Pulse response checking in each power cycle (3 cycles)
SPI checkout test	Write and read to LArASIC register
Charge pulse direct to input	To check that input is connected to preamplifier (rare case)
Channel pulse response checkout (pulsing from internal DAC)	• To check that output pins are proper connected with packaged pin • Baseline measurements (200mV/900mV) • Pulse response with different peaking time
Monitoring	• Check response from each channel (through test pad) • Baseline measurements (through commercial ADC) • BGR voltage measurement
BL restore test	Check the baseline after 200mV to 900mV baseline configuration and vice versa
Noise measurements	With different peaking time and buffer configuration
Full chain linearity measurements (LArASIC+ColdADC)	• Input from internal DAC • Direct input from external pulse generator • Input from test pin and through internal calibration capacitor • Gain, linearity and pedestal measurements
Cross-talk measurements	Cross-talk between each channel using direct input from external pulser
DAC Linearity measurements	DNL/INL of DAC with different gain settings
Channel pulse response with different leakage current settings	Baseline measurements and channel pulse response
Pulser response with different gain settings	Baseline measurements and channel pulse response
Pole-zero cancellation test	Measure the P-Z of each channel by external pulser
Internal Calibration capacitor measurements	All 1pF on-board caps are calibrated with LCR meter to measure the internal cap

Dual-DUT Test Board

- FM + Test Motherboard + 2 DUTs
  - Can characterize LArASIC thoroughly
  - The assembly will be submerged in LN2
- Interface:
  - Data is readout through UDP interface of Dual FPGA mezzanine
  - Can be readout by WIB as well (require FW update)
- Support LArASIC/ColdADC characterization

Cold Test Setup: CTS





QC Procedures

- Python script has been used to characterize the LArASIC
- Operators need to enter the Temp. and chips #

```
temperature = "RT"

FE_chip_ID="FEChip_P5B_35"          # Socket 0
FE_chip_ID_1="FEChip_P5B_36"        # Socket 1
```

- Run 'QC_DUAL_DUT_test.bat'

```
:: socket 0

python FE_adc_init.py                   0

python FE_ADC_Power.py                  0

python FE_parameter_test.py             0 0

python FE_baseline_restore_test.py      0

python adc_test_cfg.py                  CMOS SDC_OFF DB_OFF Single-Ended 16 SHAinput 0 0
python FE_Channel_Response_all.py       30us 14mVfC PLS_DIS 200mV BUF_OFF DC disable SDD_OFF 0

python adc_test_cfg.py                  CMOS SDC_OFF DB_OFF Diff 16 SHAinput 0 0
python FE_Channel_Response_all.py       30us 14mVfC PLS_DIS 200mV BUF_OFF DC disable SDD_ON 0

python adc_test_cfg.py                  CMOS SDC_OFF DB_OFF Single-Ended 16 SHAinput 0 0
python FE_Channel_Response_EX_pulse_FPGA_DAC.py  20us 14mVfC PLS_DIS 200mV BUF_OFF DC disable SDD_OFF 0

python FE_gain_measure_acq.py 05us 14mVfC PLS_EN  200mV BUF_OFF DC Internal SDD_OFF False 0
python FE_gain_measure_acq.py 10us 14mVfC PLS_EN  200mV BUF_OFF DC Internal SDD_OFF False 0
python FE_gain_measure_acq.py 20us 14mVfC PLS_EN  200mV BUF_OFF DC Internal SDD_OFF False 0
python FE_gain_measure_acq.py 30us 14mVfC PLS_EN  200mV BUF_OFF DC Internal SDD_OFF False 0

python FE_gain_measure_acq.py 05us 14mVfC PLS_EN  900mV BUF_OFF DC Internal SDD_OFF False 0
python FE_gain_measure_acq.py 10us 14mVfC PLS_EN  900mV BUF_OFF DC Internal SDD_OFF False 0
python FE_gain_measure_acq.py 20us 14mVfC PLS_EN  900mV BUF_OFF DC Internal SDD_OFF False 0
python FE_gain_measure_acq.py 30us 14mVfC PLS_EN  900mV BUF_OFF DC Internal SDD_OFF False 0
python FE_gain_fit_plot.py               BUF_OFF SDD_OFF 0

python FE_noise_acq_all.py              20us 14mVfC PLS_DIS 200mV BUF_OFF DC disable SDD_OFF 0

python Dual_dut_QC_pdf.py               0
```

- For a single chip run, it will execute around 8-9 tests and generate a single PDF.
- Also saves all the test results into .csv file
- One chip test take around ~7 minutes (Dual chip take ~14 min)

Generated Summary of LArASIC QC (1st Page)

LArASIC Test Summary

Date & Time: 2022-01-14 12:33:49 — Temperature: LN

ColdADC Chip ID: ColdADC_P2_60 — Board ID: DUAL_DUT

FE Chip ID: FEChip_P5B_42

Summary:

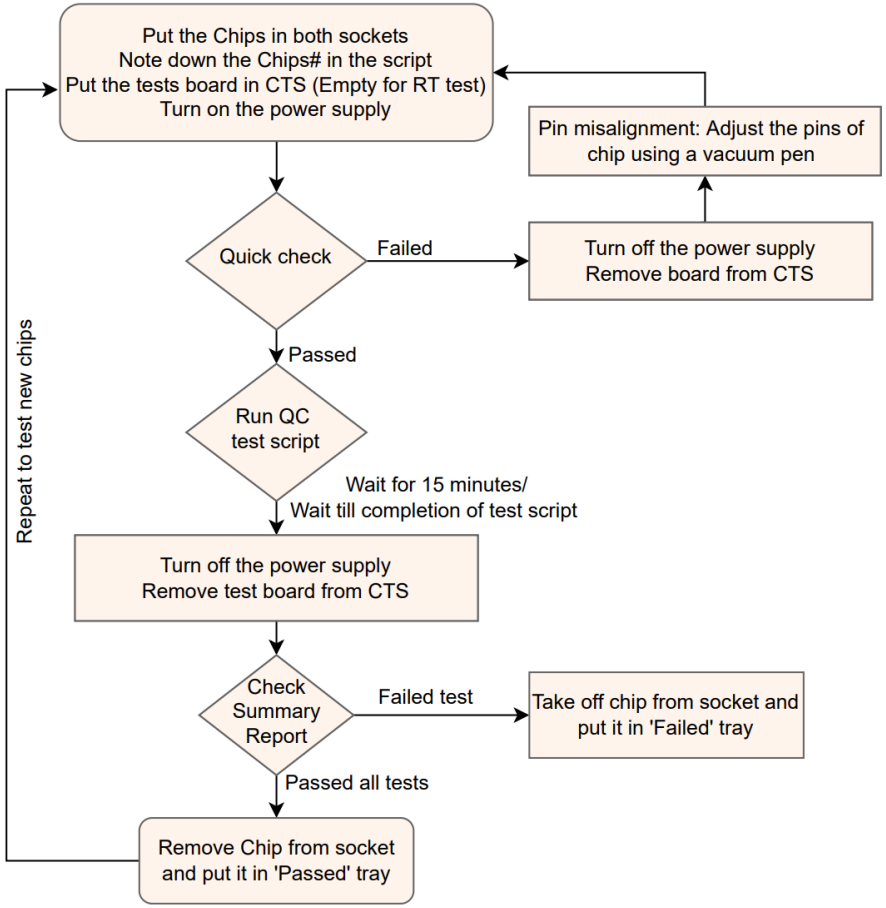
Power Measurement	Passed
FE parameter measurement	Passed
BL Restore Test	Passed
Channel Response (Internal DAC) @SDD_OFF	Passed
Channel Response (Internal DAC) @SDD_ON	Passed
Channel Response (Ext Pulse) @	Passed
FE gain plot (DAC pulsing)	Passed
FE Noise	Passed

➢ Database Interface

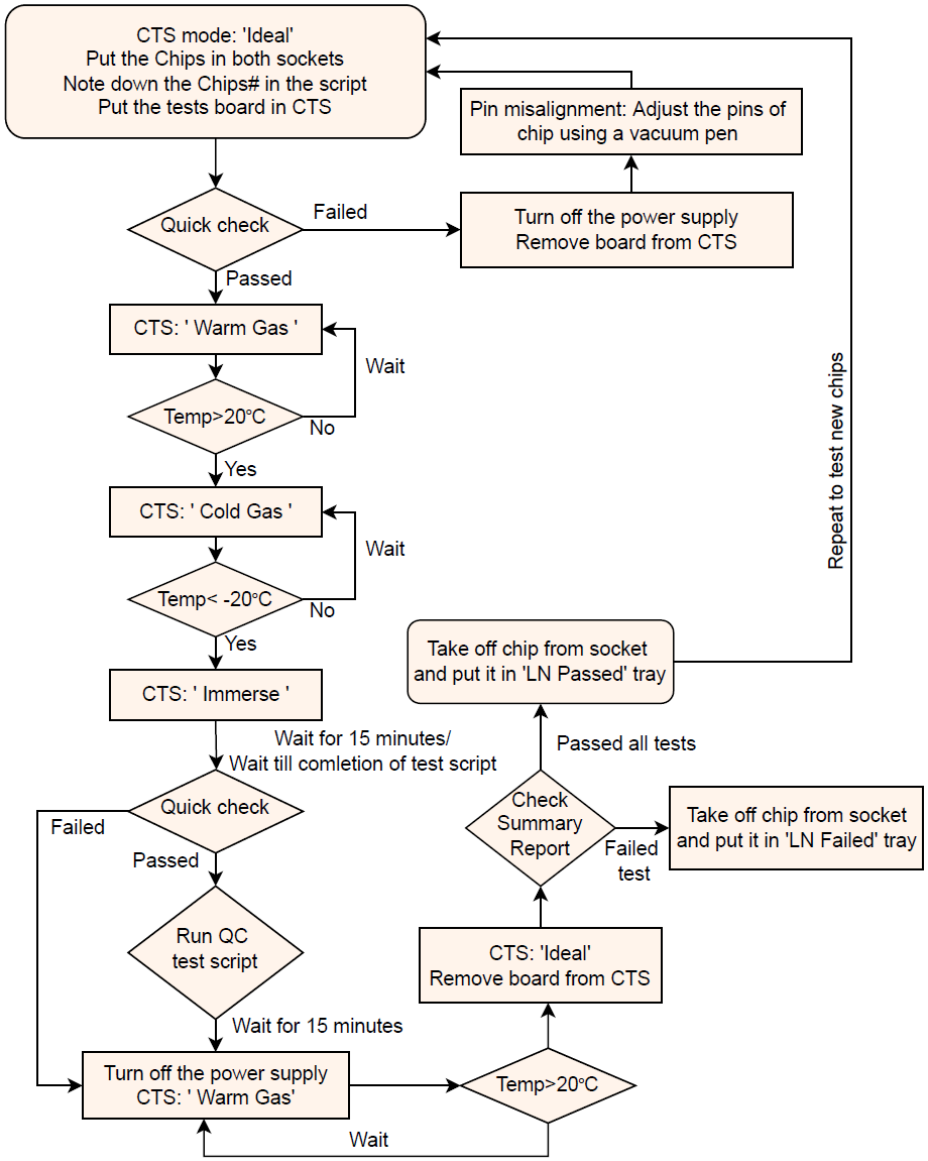
- All test data will be stored in BNL local database used in ProtoDUNE-I (Later we can store/transfer to the direct hardware database)
- Plan to develop a database template which can help user to monitor and archive the QC test results

QC Procedures

RT Test



Cold/LN2 Test



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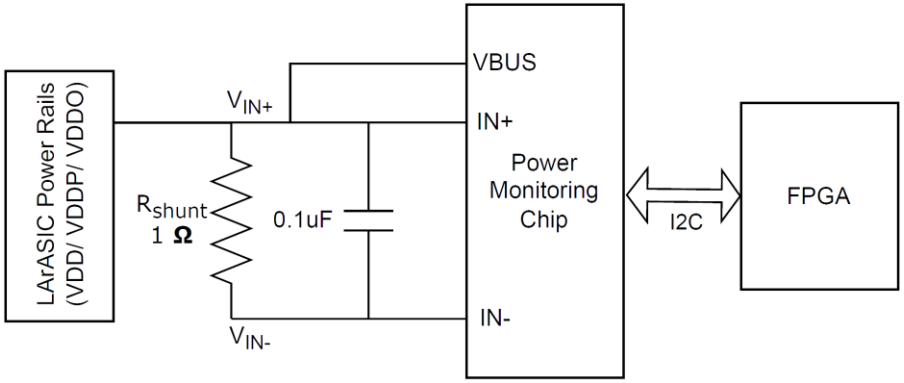
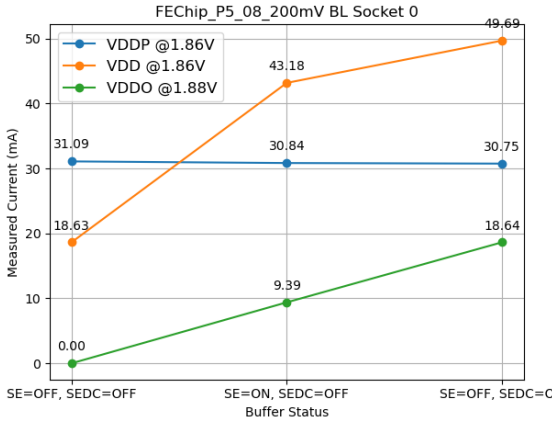
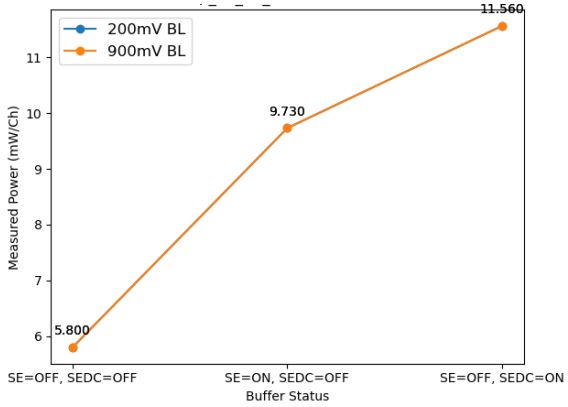
Power Measurements



- Power monitoring chip is used to monitor voltage/current/power of LArASIC power rails
- Measurement at different LArASIC buffer settings
- LArASIC power rails: VDDP, VDD, VDDO
- ColdADC power rails: VDDA2P5, VDDD2P5, VDDIO, VDDD1P2
- Save results on .csv file

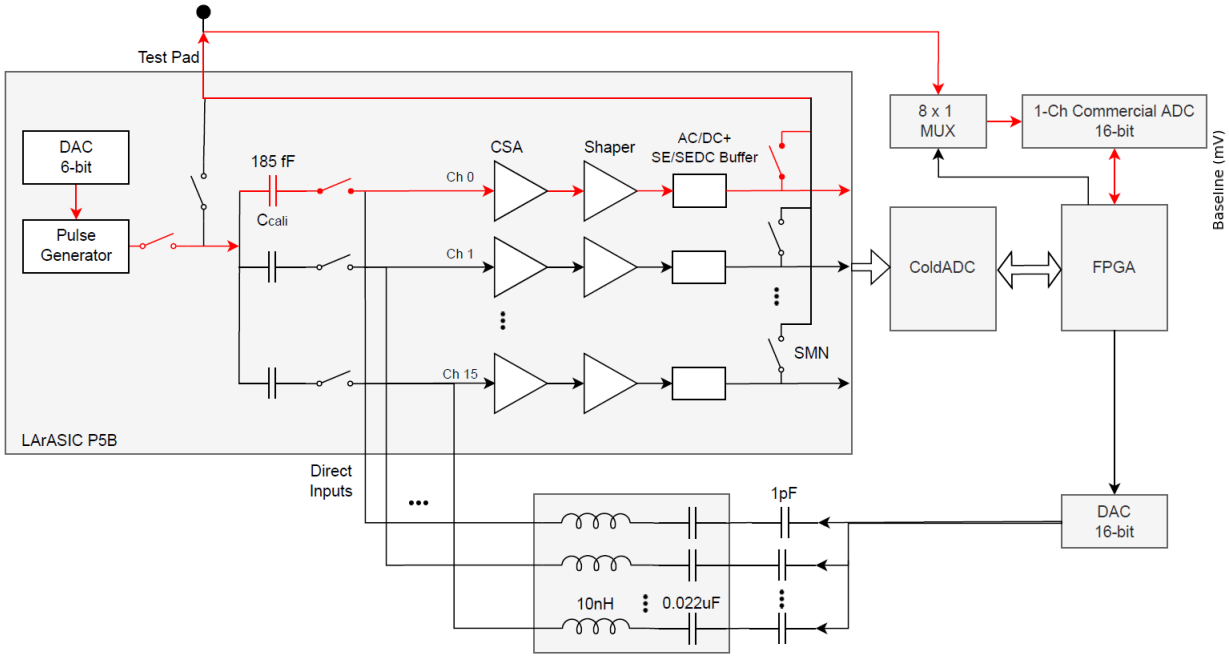




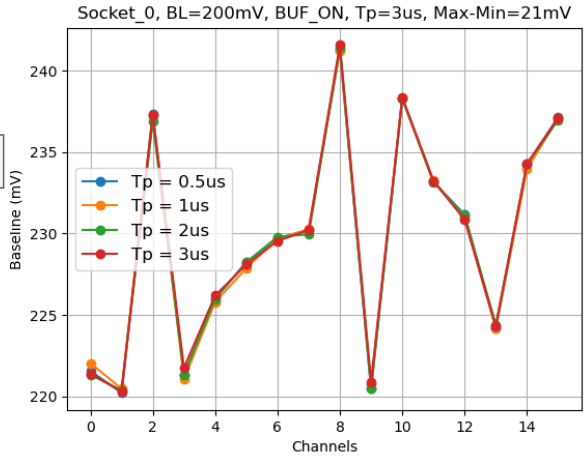
LArASIC P5B #08 @RT

SE=OFF SEDC=OFF	**900 mV (BL)**	
Power Rail	Voltages (V)	Current (mA)
VDDP	1.86	31.11
VDD	1.86	18.63
VDDO	1.88	0
Power (mW/Ch)	5.8	
SE=ON SEDC=OFF	**900 mV (BL)**	
Power Rail	Voltages (V)	Current (mA)
VDDP	1.86	30.85
VDD	1.86	43.2
VDDO	1.87	9.4
Power (mW/Ch)	9.73	
SE=OFF SEDC=ON	**900 mV (BL)**	
Power Rail	Voltages (V)	Current (mA)
VDDP	1.86	30.75
VDD	1.86	49.71
VDDO	1.87	18.65
Power (mW/Ch)	11.56	
SE=OFF SEDC=OFF	**200 mV (BL)**	
Power Rail	Voltages (V)	Current (mA)
VDDP	1.86	31.09
VDD	1.86	18.63
VDDO	1.88	0
Power (mW/Ch)	5.79	
SE=ON SEDC=OFF	**200 mV (BL)**	
Power Rail	Voltages (V)	Current (mA)
VDDP	1.86	30.84
VDD	1.86	43.18
VDDO	1.87	9.39
Power (mW/Ch)	9.73	
SE=OFF SEDC=ON	**200 mV (BL)**	
Power Rail	Voltages (V)	Current (mA)
VDDP	1.86	30.75
VDD	1.86	49.69
VDDO	1.87	18.64
Power (mW/Ch)	11.56	

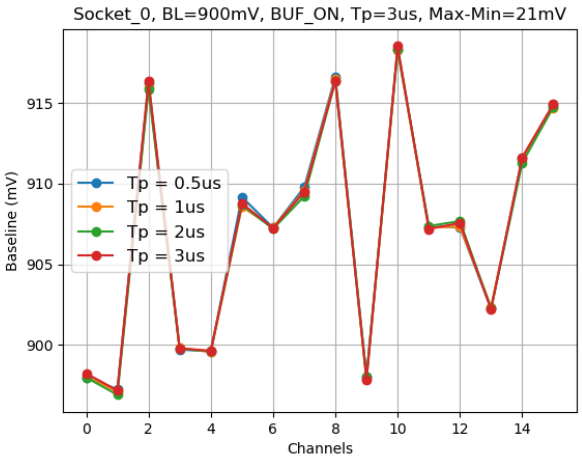
LArASIC Baseline Measurements



200 mV BL @LN2

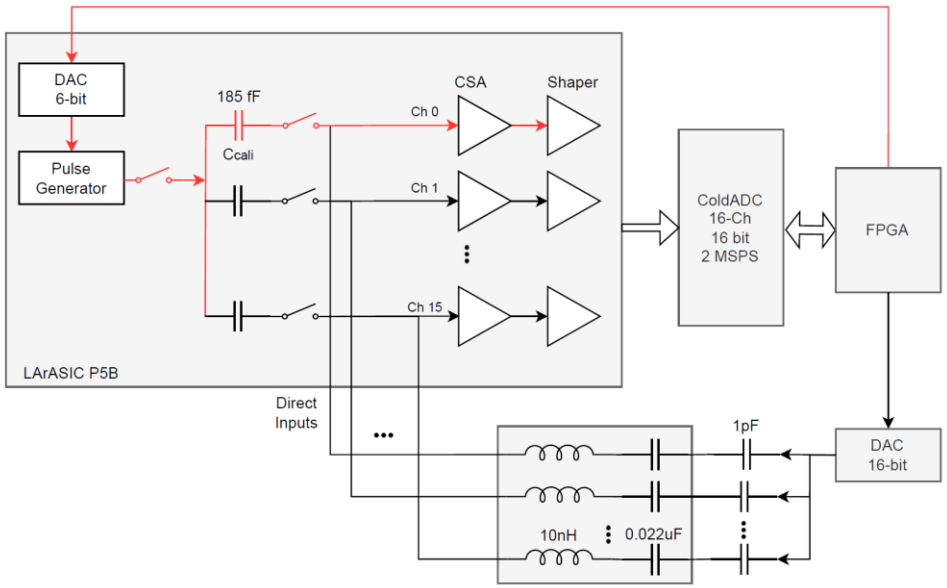


900 mV BL @LN2

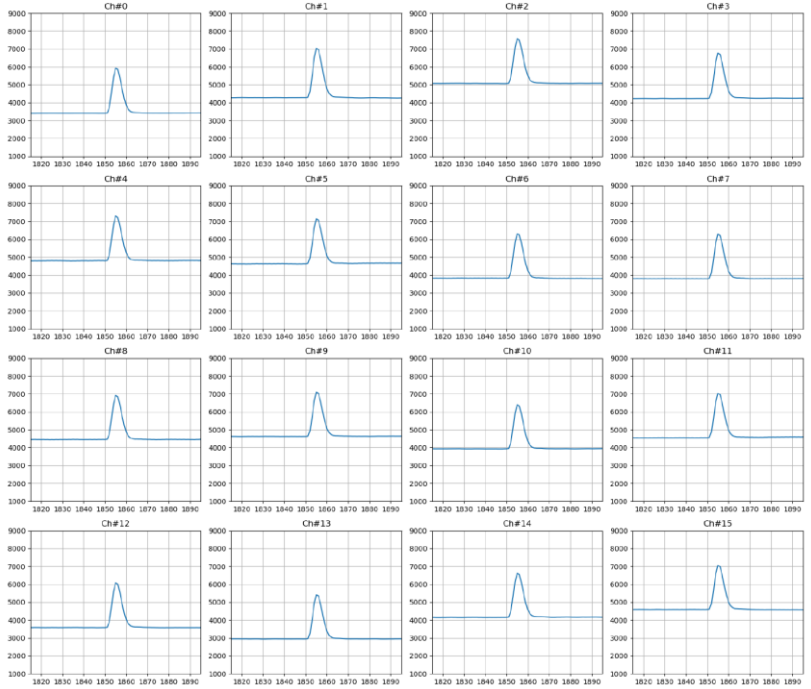


- Commercial ADC: 14 bit, 4.5 MSPS is used
- Baseline measurements from LArASIC monitoring pin and through commercial ADC for all 16 channels (to bypass ColdADC)
- Band gap reference voltage (VBGR) and temperature sensor voltage is also measured
- FE settings:
  - Tp = 0.5/1/2/3us , Pulse = Disable, Gain = 14 mV/fC , RQI = 500 pA, BL = 200 mV / 900mV, Buffer = OFF, SEDC = OFF
- Baseline measurement results are consistent with the previous measurement done by multimeter on the LArASIC single chip test board

LArASIC Channel Pulse Response Checkout



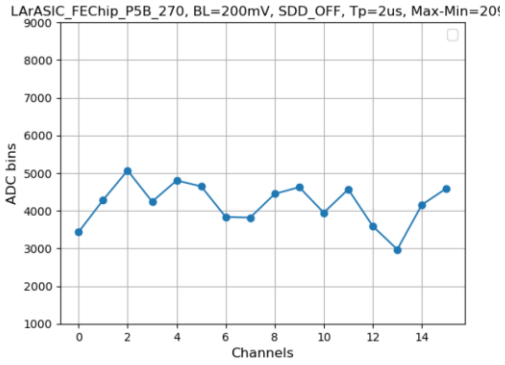
@ LN2, Tp=2us, 200mV BL



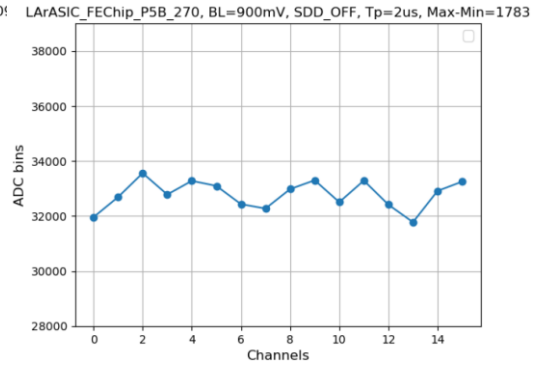
- Used FE internal DAC pulse for channel pulse response checkout
- Plots of pulse responses for all 16 channels
- Plots of baseline dispersion for all 16 channels (FE Input disable)
- Different configuration settings are used:
  - Baseline: 200 mV/900mV
  - SE Buffer condition: BUF_ON/BUF_OFF
  - Peak time: 0.5/1/2/3 us

Baseline dispersion (FE LArASIC P5B + ColdADC P2)

200mV BL



900mV BL



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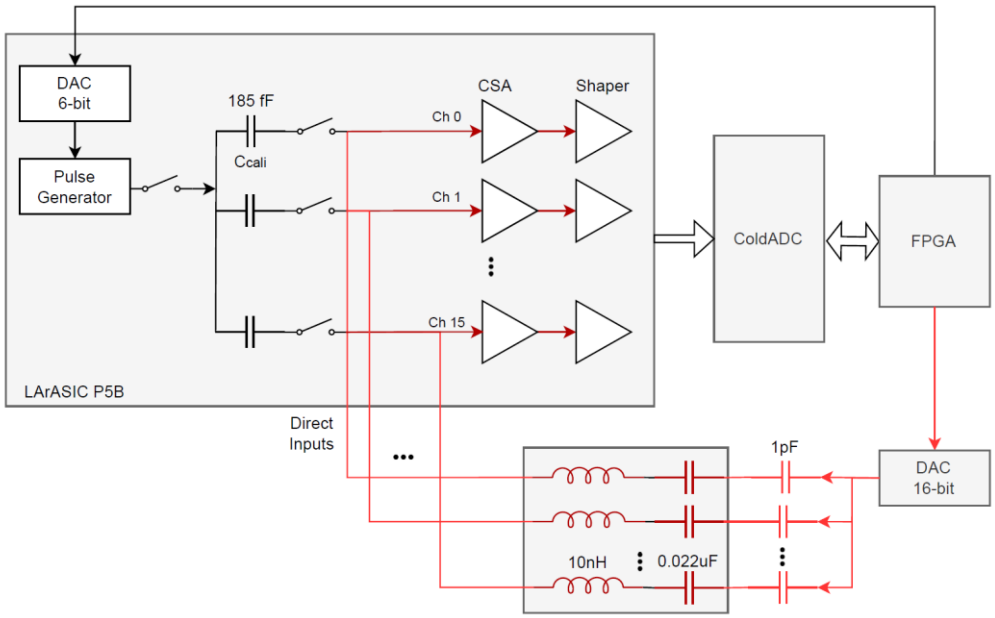
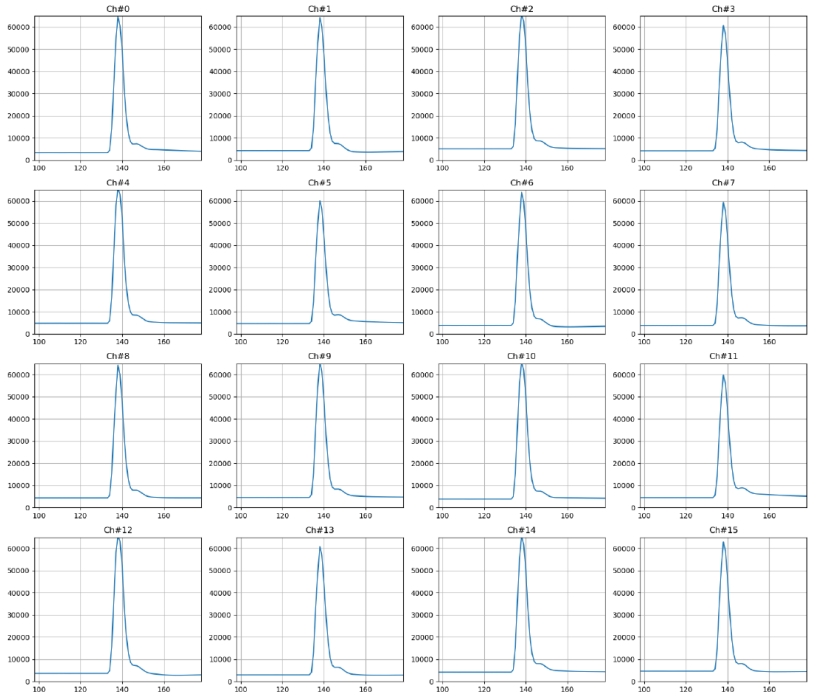
LArASIC Channel Pulse Response
(External Pulser)

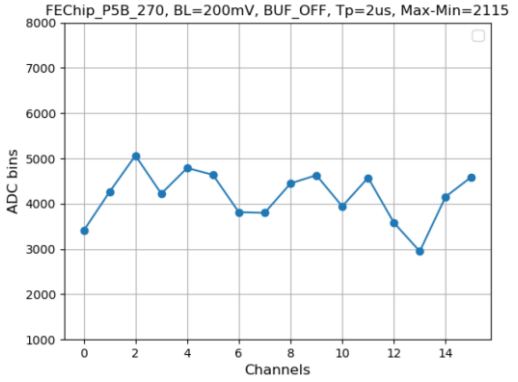


@ LN2, Tp=2us, 200mV BL



Baseline dispersion (FE LArASIC P5B + ColdADC P2)

200mV BL



- Used External DAC pulse for channel pulse response checkout
- Useful to check the proper wire connections between the packaged pin and die
- Plots of pulse responses for all 16 channels
- Plots of baseline dispersion for all 16 channels (FE Input disable)
- Different configuration settings are used:
  - Baseline: 200 mV
  - SE Buffer condition: BUF_ON/BUF_OFF
  - Peak time: 2 us

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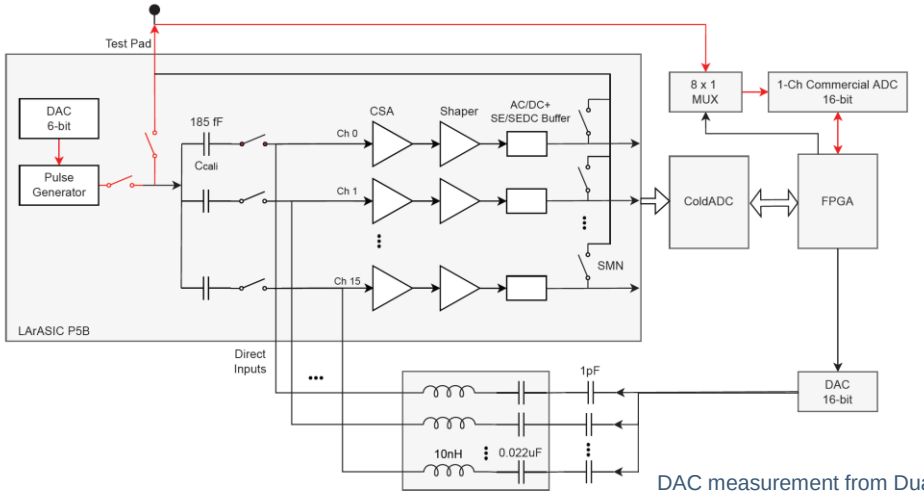
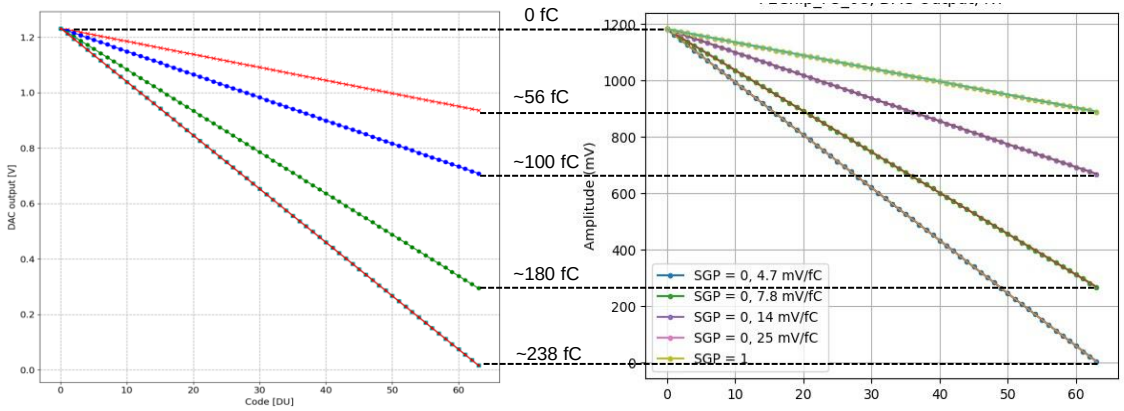
DAC Linearity Measurement

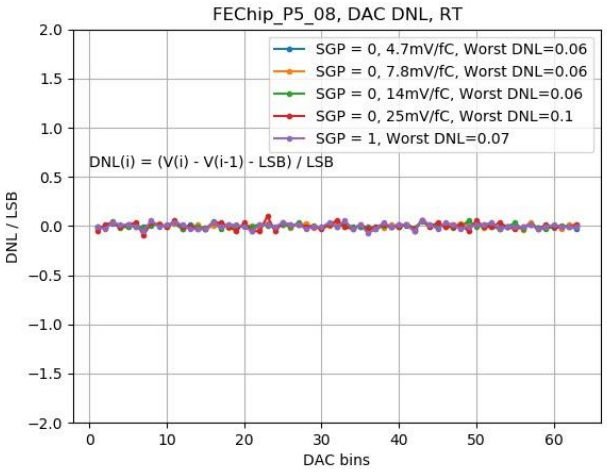


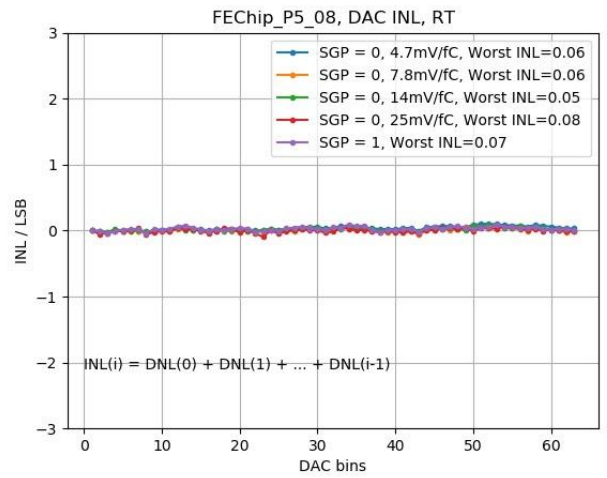
DAC Simulation @ RT



DAC measurement from Dual-DUT test board
LArASIC P5B @ RT

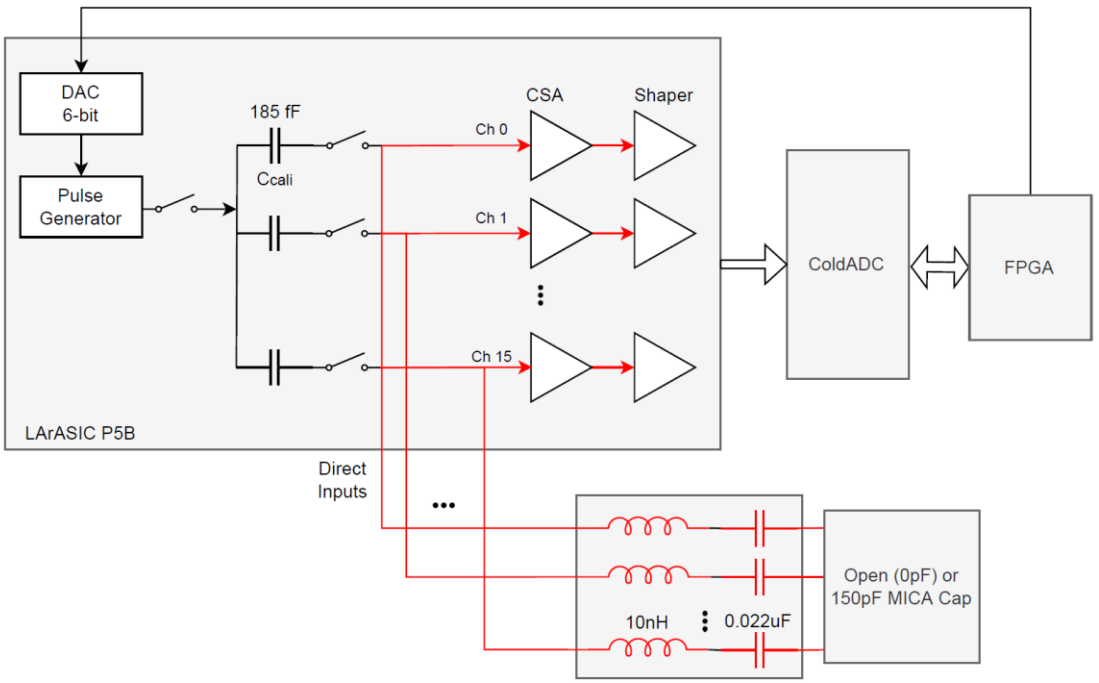
LArASIC P5B @ RT



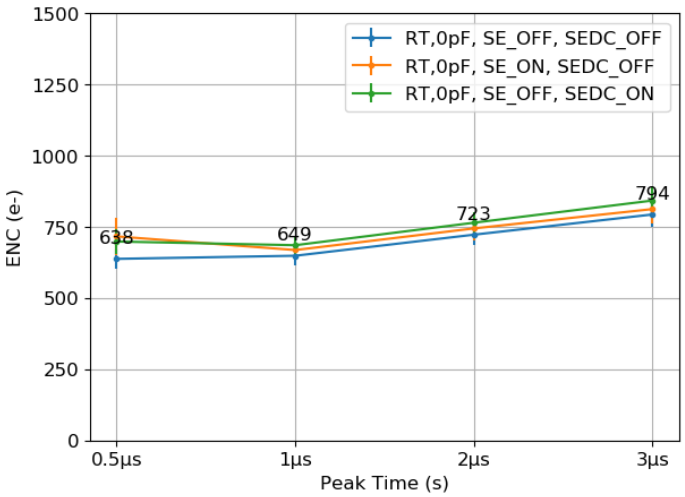


- The DAC performance can be characterized on the Dual-DUT test board
- Commercial ADC, 14 bit is used to digitize DAC output
- Plots of DAC amplitude with different gain settings
  - Gain: 4.7/7.8/14/25 mV/fC and SGP=1
- DAC has acceptable measured DNL of < 0.1 LSB and INL of < 0.08 LSB

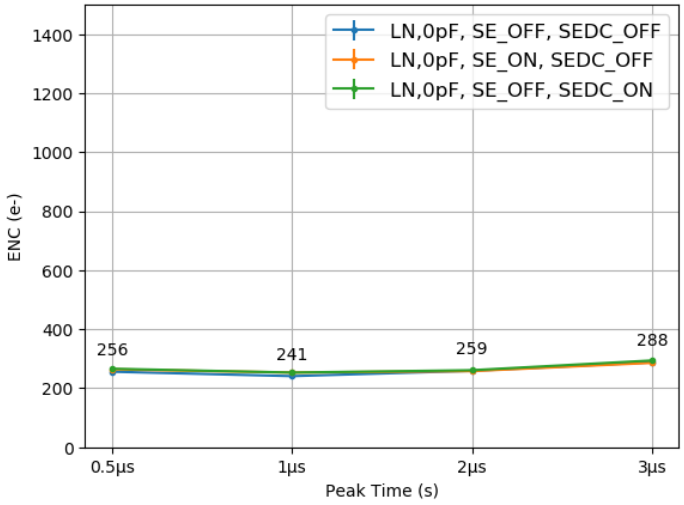
LArASIC Noise Measurements



@RT, Cd= 0pF



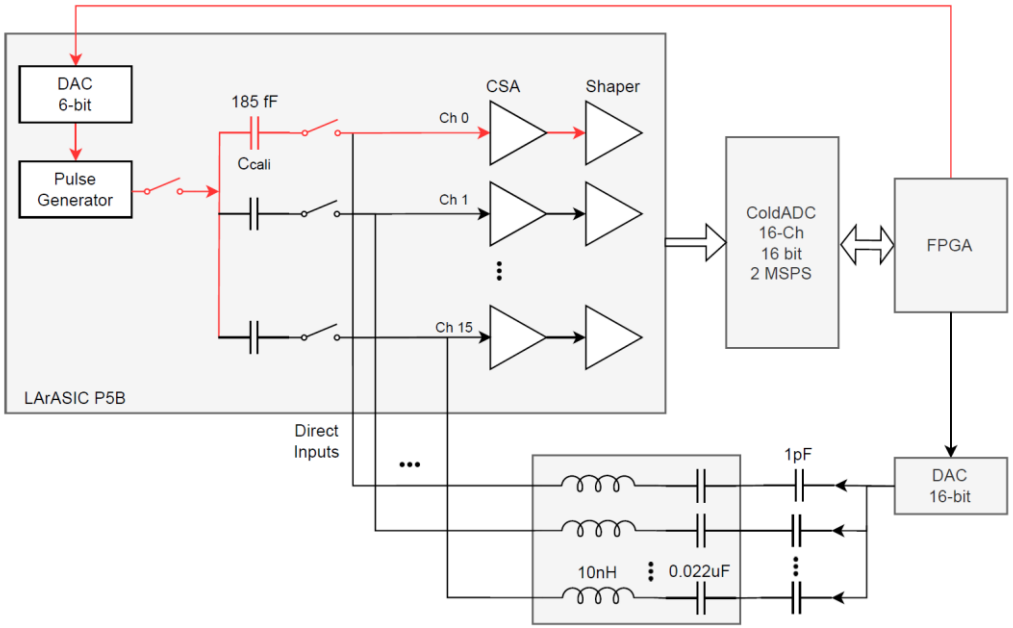
@LN2, Cd= 0pF



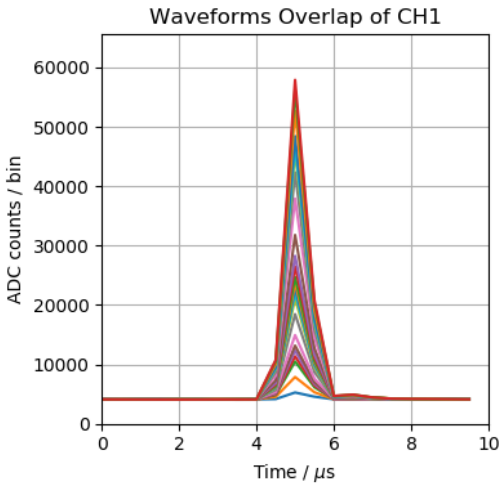
- The noise of LArASIC can be characterized on the Dual-DUT test board
- P5B LArASIC and P2 ColdADC full chain test board assembly
  - P5B LArASIC + P2 ColdADC test board
- Test settings:
  - LArASIC: 200 mV BL, 14 mV/fC gain, 500 pA RQI, 0 pF Cd, Single-ended/Diff
  - ColdADC: SDC off, DB off, Single-ended/Diff
- Note: These are the preliminary noise results as QC setup and test board are not capable of measuring precise noise

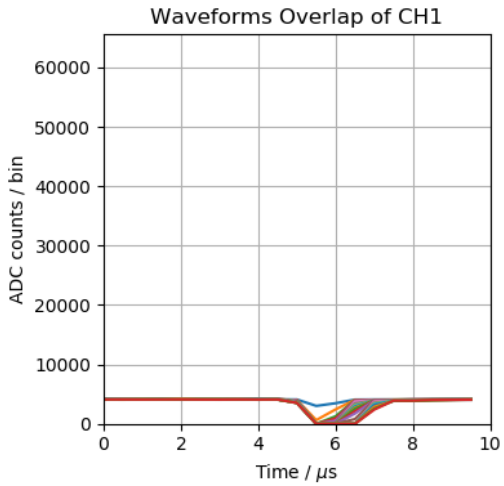
LArASIC Linearity Measurement (1)

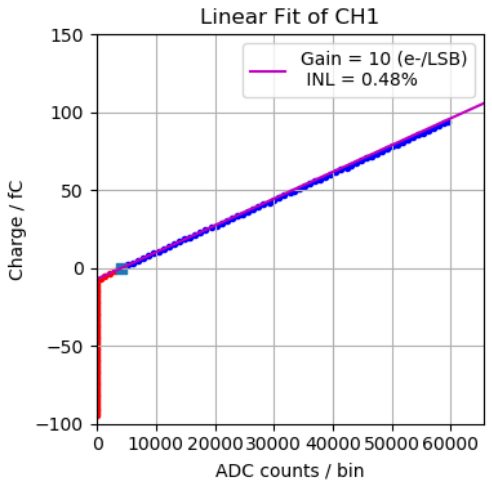
Using Internal pulser



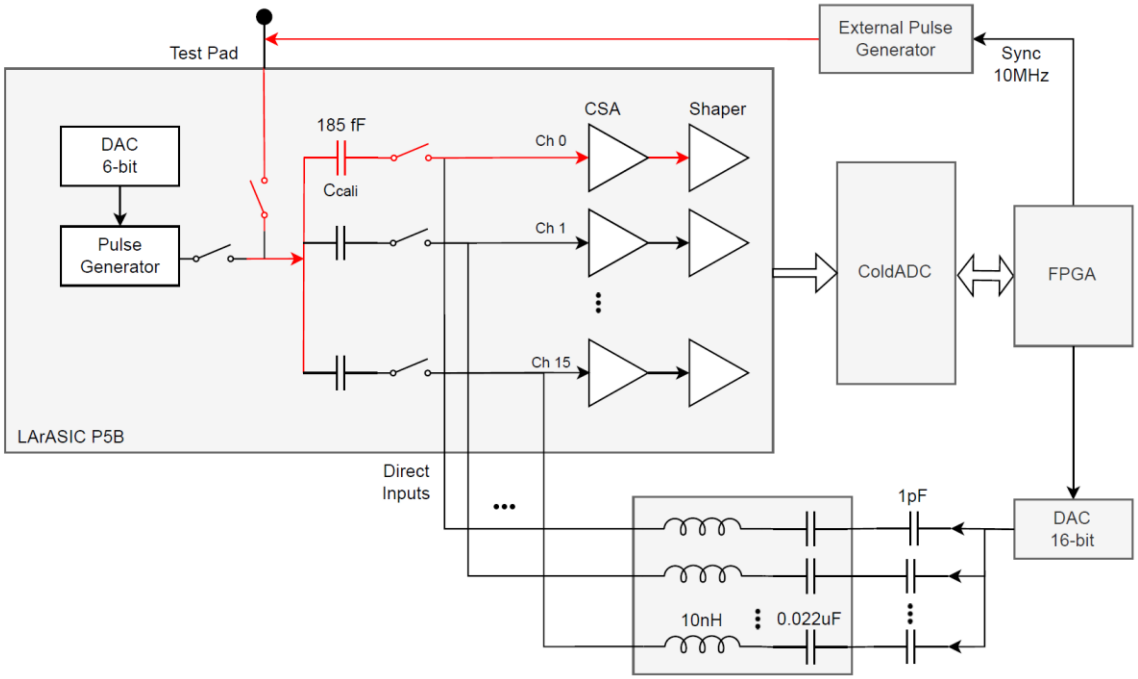
- Full chain linearity is measured which includes the nonlinearities of
  - Internal DAC + LArASIC P5B+ColdADC P2
- Settings:
  - FE : BL=200mV, Gain =14mV/fC, Tp=2us,
  - FE Buffer: SE=OFF, SEDC= OFF
  - ColdADC: CMOS Ref, SDC_OFF, DB_OFF, Single-Ended
- Linearity measurements for the different combinations of BL (200mV/900mV) and peaking time (0.5us/1us/2us/3us)





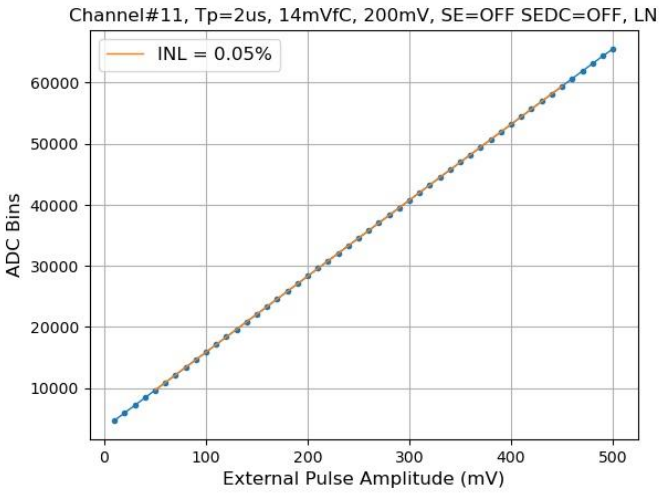


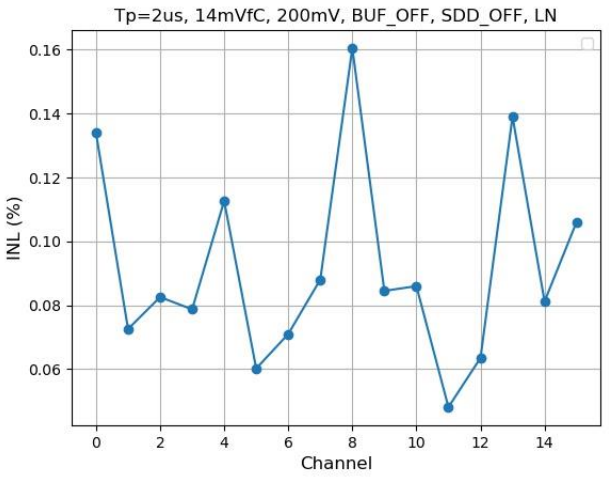
LArASIC Linearity Measurement (2)



Using external pulser

(Through test pin and internal calibration cap)





- For the precise linearity measurements, we used the external pulse generator and also implemented phased delay logic for the precise amplitude peak detection
- One by one channel was enabled to avoid cross-talk between individual channels
- Synchronized external pulse generator using FPGA 10 MHz clock
- Pulse setting: Freq: 1kHz, Amplitude = 10mV-500mV, Pulse width=50us, Edge= 5ns, Phase=variable (Fixed at maximum amplitude after calibration)
- Full chain linearity: LArASIC P5B + ColdADC P2
- FE : BL=200mV, Gain =14mV/fC, Tp=2us,
- ColdADC: CMOS Ref, SDC_OFF, DB_OFF, Single-Ended
  - Internal DAC + LArASIC P5B+ColdADC P2

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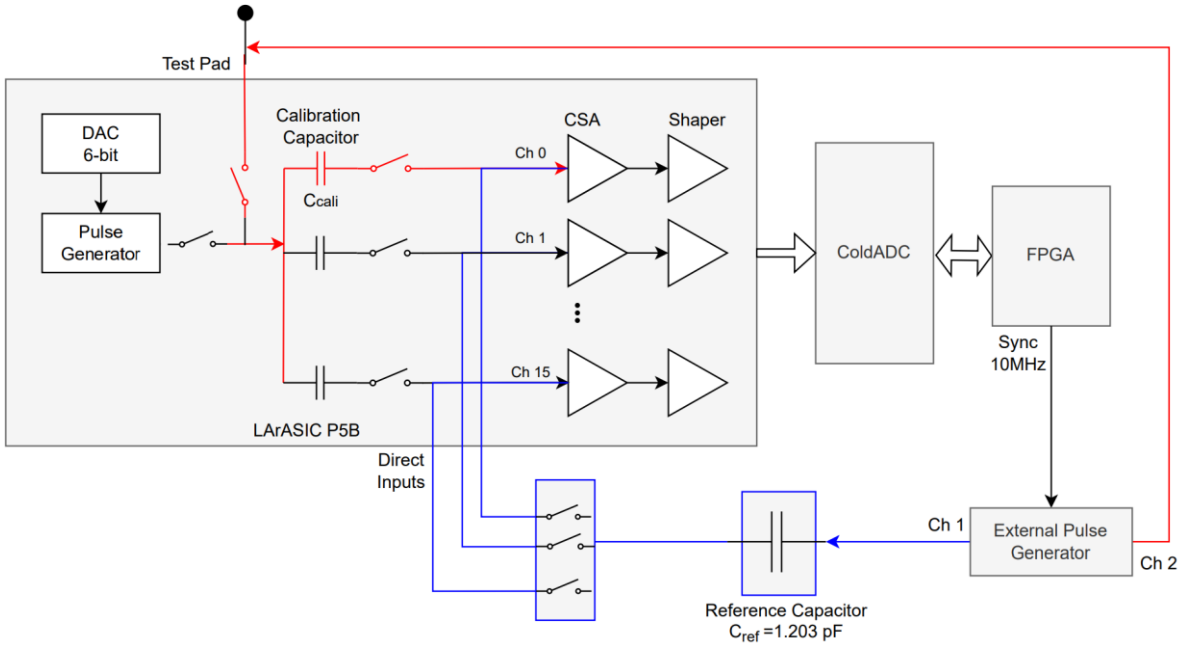
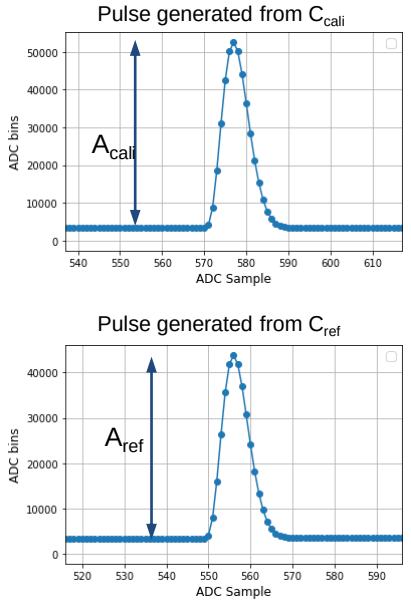
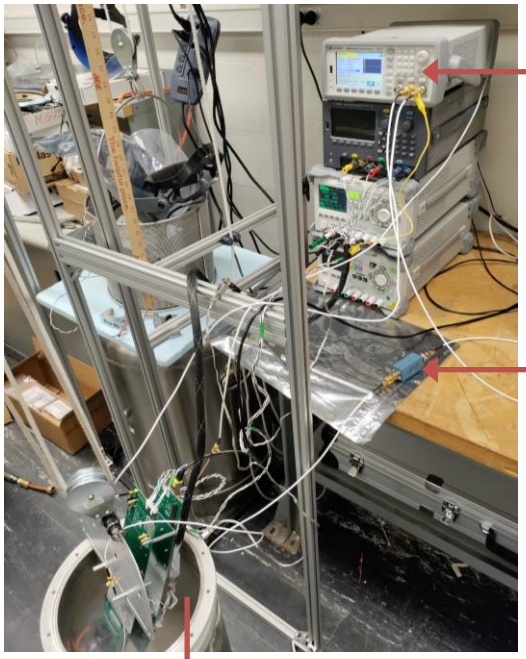
Calibration Capacitor Measurements

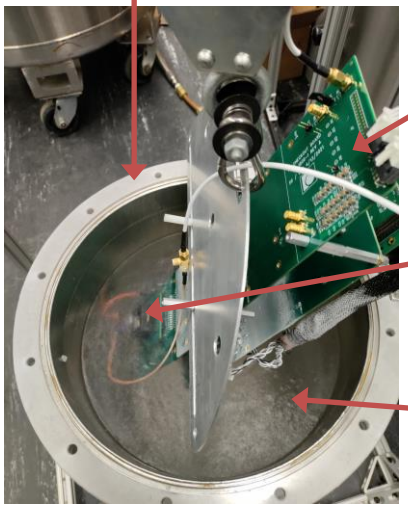


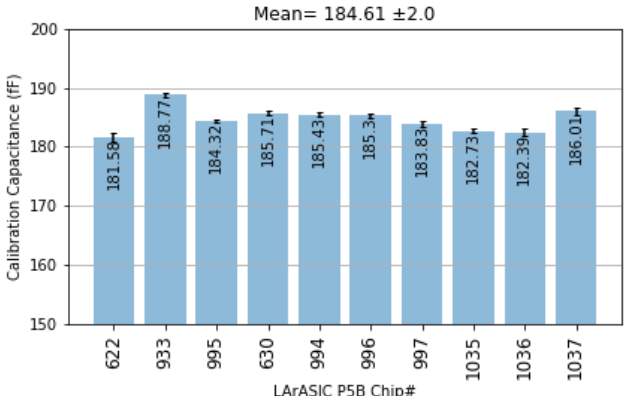


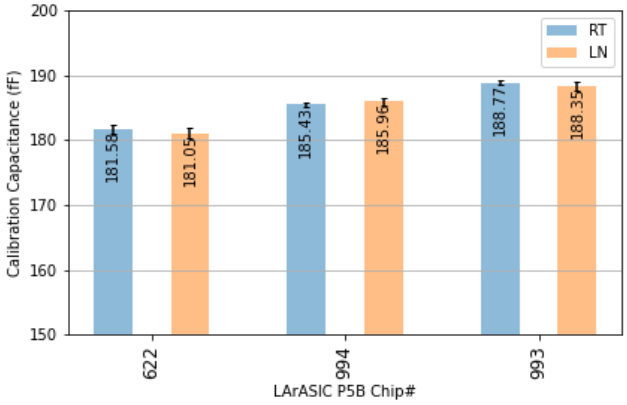
- The current Dual-DUT board doesn't have the capability to measure the calibration capacitor
- Single test chip test boards have been used to measure the calibration cap
- C_{ref} =1.203 pF is calibrated by standard 1.0pF and LCR meter
  - C_{ref} is always put in room temp.
- Since input pulse amplitude is constant,
  - $C_{cali} : C_{ref} = A_{cali} : A_{ref}$

Calibration Capacitor Measurements





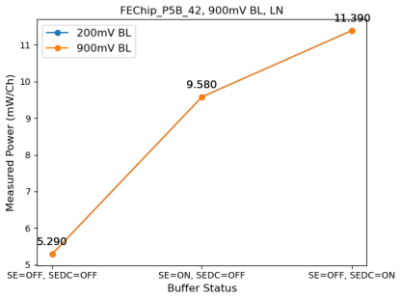




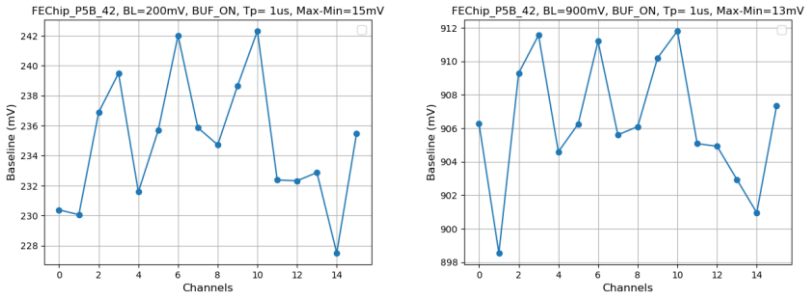
- Integrated Test Capacitor Measurements of LArASIC P5B
  - Very little variation among different channels in the same chip (~0.2%)
  - Observed slightly variation among different packaged chips in the same batch (~1%)
  - Negligible variation in the capacitance at RT and Cold (LN2) temperature in the same chip (~0.1%)
- In future QC test-board design, we will add such a facility to measure calibration capacitor

QC Results

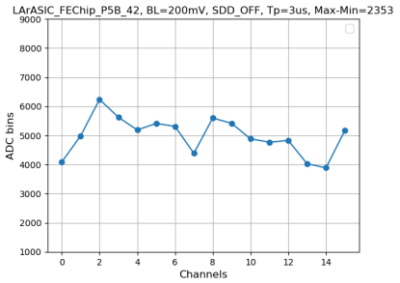
Power Consumption



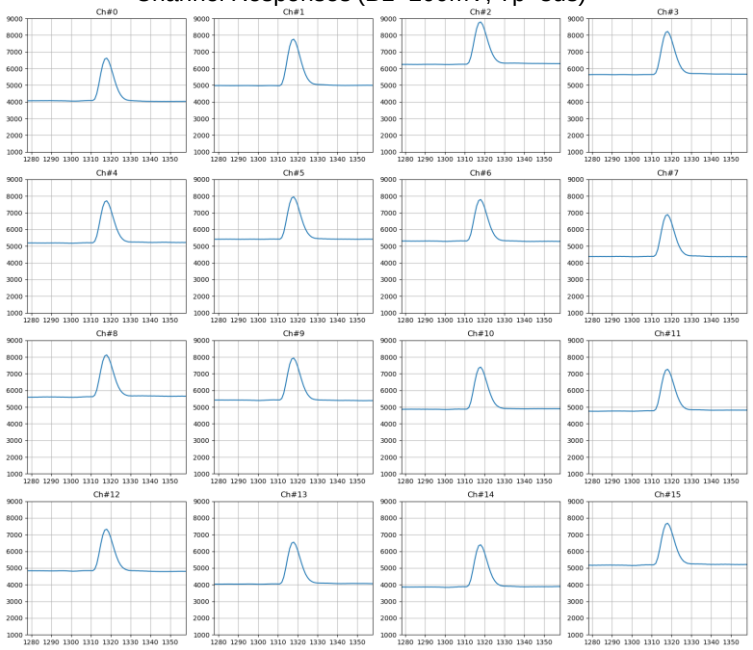
BL measurements (using commercial ADC)



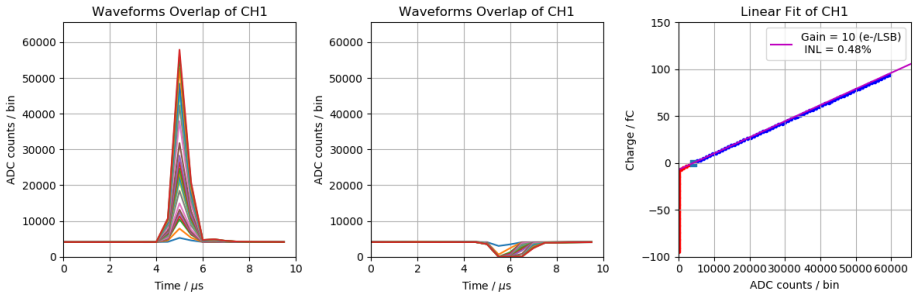
BL measurements (using ColdADC)



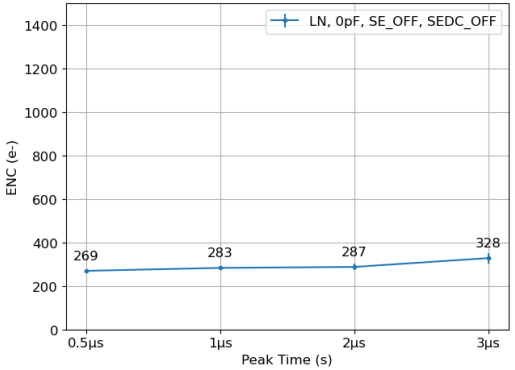
Channel Responses (BL=200mV, Tp=3us)



Gain, Linearity Measurements



Noise Measurements, (0pF)



The acquired results satisfy all the required DUNE specifications for LArASIC quality control.

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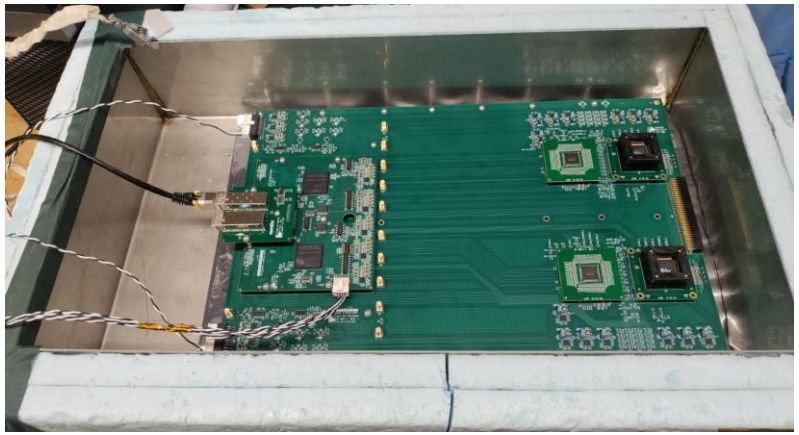
LArASIC P5B: Yield

- We have finished the testing of all LArASIC P5B chips at RT
- Cold screening of LArASIC P5B is going on
  - Two CTS are being used for cold screening

RT test setup



Cold test setup

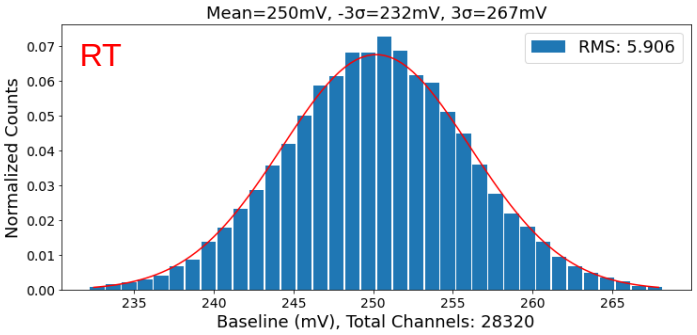
LArASIC Chips	Temp.	Tested Chips#	Good # (All channels are normal)	Yield
P5B	RT	1786	1767	~99.0 %
P5B	Cold/LN2	617	613	~99.35 %

- At RT: 19 chips have failed at RT
- At LN2: Four chips have failed at LN2 which works fine at RT

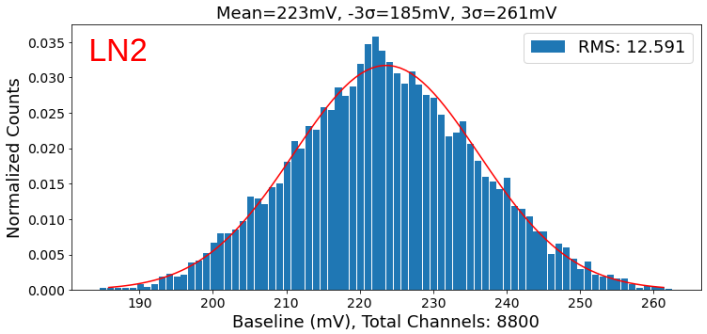
Preliminary Data Analysis

- Number of channels
  - @RT: 28320
  - @LN2: 8800

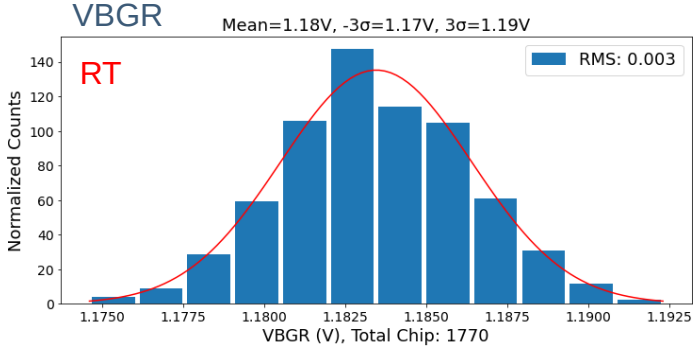
BL, 200mV



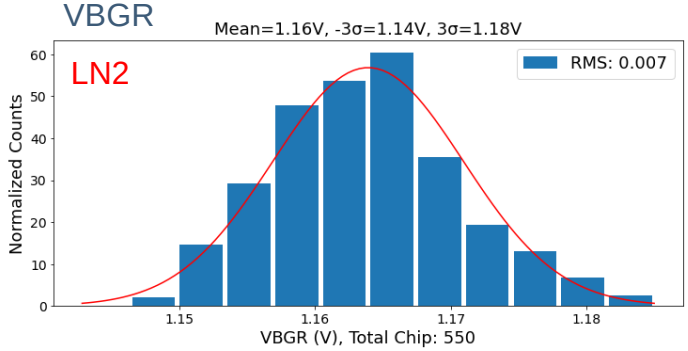
BL, 200mV



VBGR



VBGR



LArASIC Parameter	Mean (RT/LN2)	SD (RT/LN2)
BL, 200mV (mV)	250 / 223	5.9 / 12.6
BL, 900mV (mV)	933 / 903	4.04 / 8.65
Power, (mW/Ch)	6.1 / 5.37	0.13 / 0.19
BGR voltage(V)	1.18 / 1.16	0.003 / 0.007
Noise, Tp=0.5us (ENC)	622.29 / 281.94	34.9 / 41.21
Noise, Tp=1us (ENC)	686.50 / 280.58	42.3 / 32.68
Noise, Tp=2us (ENC)	711.67 / 279.61	48.9 / 35.82
Noise, Tp=3us (ENC)	766.51 / 319.59	56.16 / 45.81
Linearity, Tp=1us (INL)	0.29 / 0.51	0.15 / 0.4

Summary

- In QC setups for LArASIC characterization for ProtoDUNE-II, a Dual-DUT board has been used for the parallel testing of two chips in a single thermal cycle.
- This successful attempt of systematic testing of LArASIC characterization is intended to emphasize the preliminary technical steps for a successful and well-structured procedure for future large-batch QA/QC production testing of LArASIC chips for cryogenic operation in DUNE.
- Finished the QC testing of all LArASIC P5B chips at RT
  - #1767 chips have passed the RT screening test, and achieved yield is ~99%
  - #19 chips (~1%) chips have failed at RT
    - #6 chips are completely failed, #13 chips have a unique failure issue
    - No abnormal leakage current for any QC failed channels, No ESD damaged channel so far
- The Cold screening is LArASIC P5B is going on
  - #613 chips have passed the cold screening test, and achieved yield is ~99.3%
  - #4 chips (~0.65%) have abnormal pulse responses and baseline at 200mV BL settings
  - No complete dead channels at Cold/LN2

Future R&D

- As large batches of cold chips in the future need more cold screening and to reduce thermal cycle testing time, a DUNE ASIC test (DAT) board hosting multiple chips (#8 chips) is under design and the cryogenic procedures for QC of the multichip test are being evaluated.
  - Can perform QC testing for 8x LArASIC, 8x ColdADC and 2x COLDATA at both RT and LN2 with MSU's new RTS
  - Aim for DUNE FD1 & FD2 ASIC QC carried out in several test sites
- In addition, robotic designs for automated LArASIC/cold chip tests are also being considered to further reduce human interference with the QC procedure.

Thank You

Back up slides

Summary of Failed Chips

RT Failed Chips

Chip#	Comments
269	Ch#15, Control register of Ch#15 can't configure correctly, produces only default results
198	Ch#06, BL~0V for DC coupling, BL is normal for AC coupling, no pulse response
1366	All Ch, 200 mV BL settings: Pulse is bad, BL is almost 0, ~50mV
1685	Ch#01, Dead channel with Tp =2us and Tp =3us peaking time
788	Ch#05, Dead channel with Tp =3us peaking time
1027	Ch#07, Dead channel with Tp =0.5us and Tp =1us peaking time
929	Ch#12, No pulse response, 200mV is ok, 900mV BL is abnormal
1611	All Ch, BL is ok, No pulse response for any settings
967	Ch#02, Complete dead for all settings, leakage current is ok
1677	Ch#12, pulsing from the external source failed. Pin connection with die is completely open
601	Ch#0, BL is abnormal when SE buffer=OFF
1518	VDDP Bus consumes less current for any buffer settings, ~3.2mA
1387	Ch#09. BL and pulse response are abnormal
Others	Complete fail at RT, couldn't characterize it

Cold/LN2 Failed Chips

Chip#	Comments
18	13 channels has abnormal BL and pulse responses at 200mV BL settings
800	All channels has abnormal BL and pulse responses at 200mV BL settings
824	Ch#12 has abnormal BL and pulse responses at 200mV BL settings
815	BL is slightly higher than expected value at 200mV BL settings