Timing reference correction for the CMS improved Resistive Plate Chambers (iRPC)

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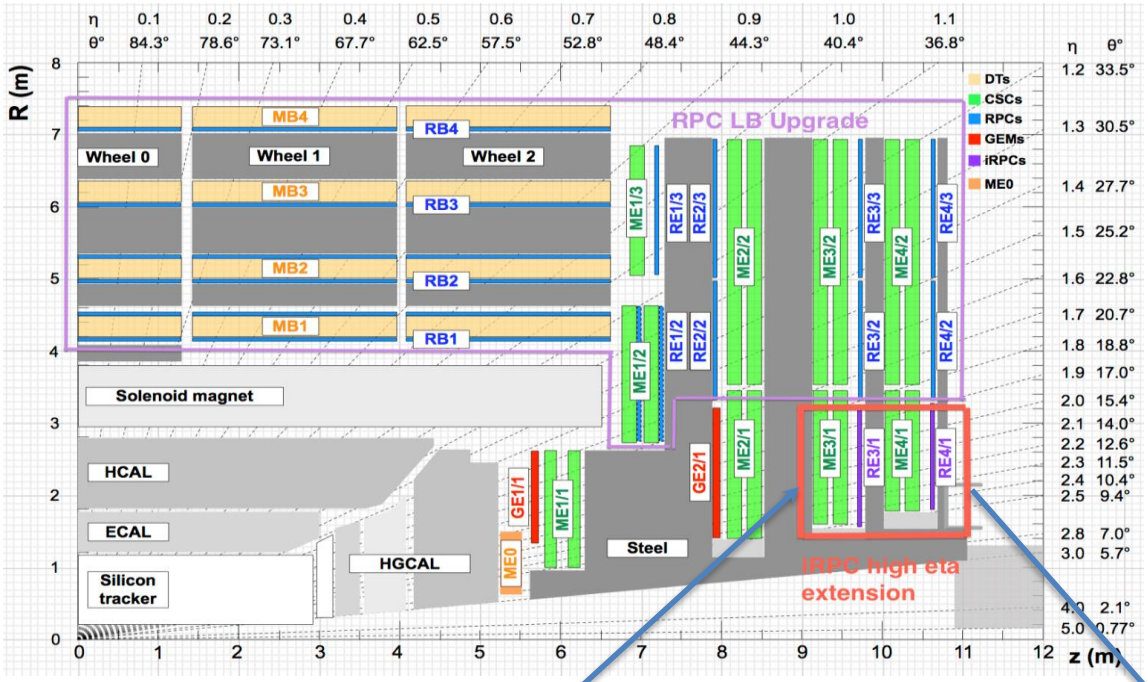
Outline

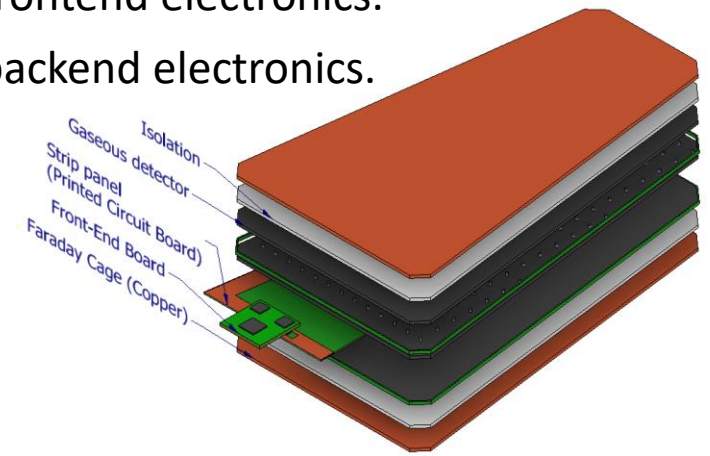
- Introduction
- iRPC timing reference issue
- Timing reference correction
- Test results
- Summary

iRPC introduction



Extend the RPC coverage up to |η | = 2.4 to increase redundancy in high eta region in stations 3 and 4
RE 3.1 and RE 4.1 Improved RPC

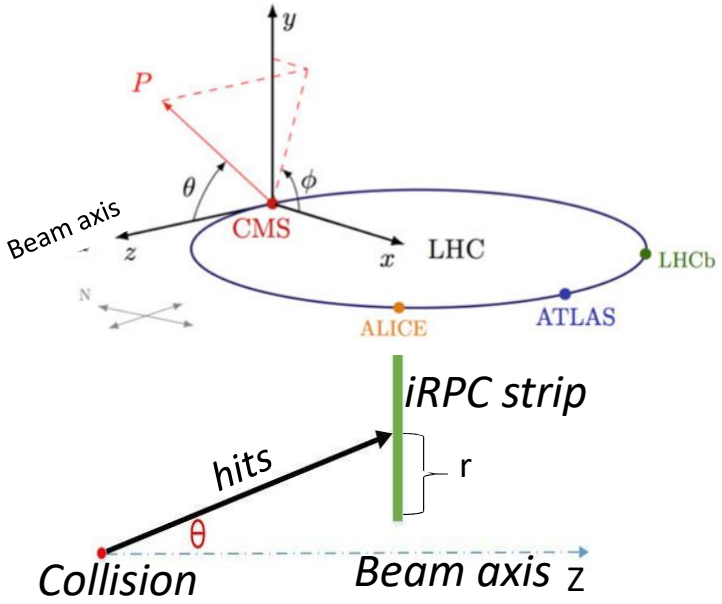
- **Main motivations/goals**:
  - Increase rate capability (2 kHz/cm^2).
  - Better time resolution for background rejection 25 ns -> 1.5 ns.
  - Better spatial resolution for tracking in r direction 40 cm-> 2 cm.
  - Improved contribution of RPCs to muon triggering in the forward region.
- **Electronics:**
  - **Two ends readout.**
  - New frontend electronics.
  - New backend electronics.

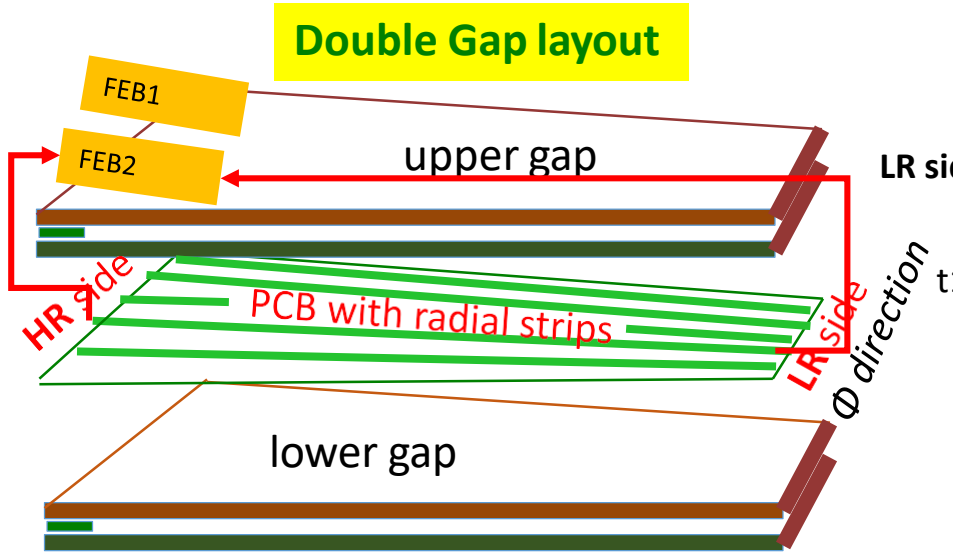


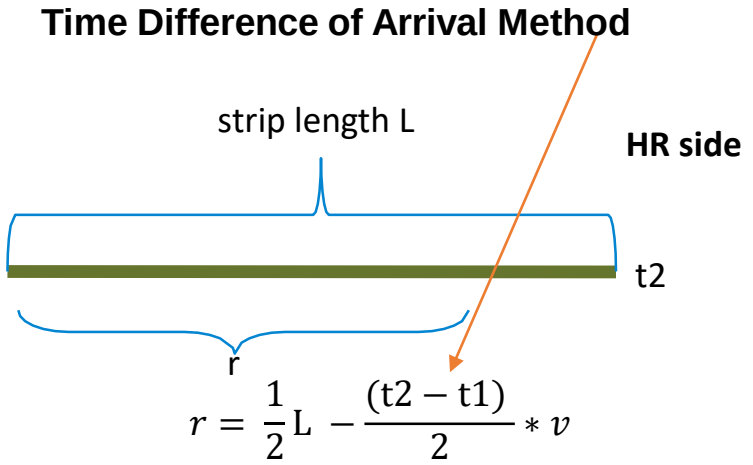
1 chamber ≈ **1.6 x 1.2 m^2 trapezoidal shape**
20° in φ ⟹ 18 chambers/disk ⟹ Total of 72 iRPC chambers

Principle of iRPC position measurement

- Two-end readout iRPC used in CMS Phase II upgrade







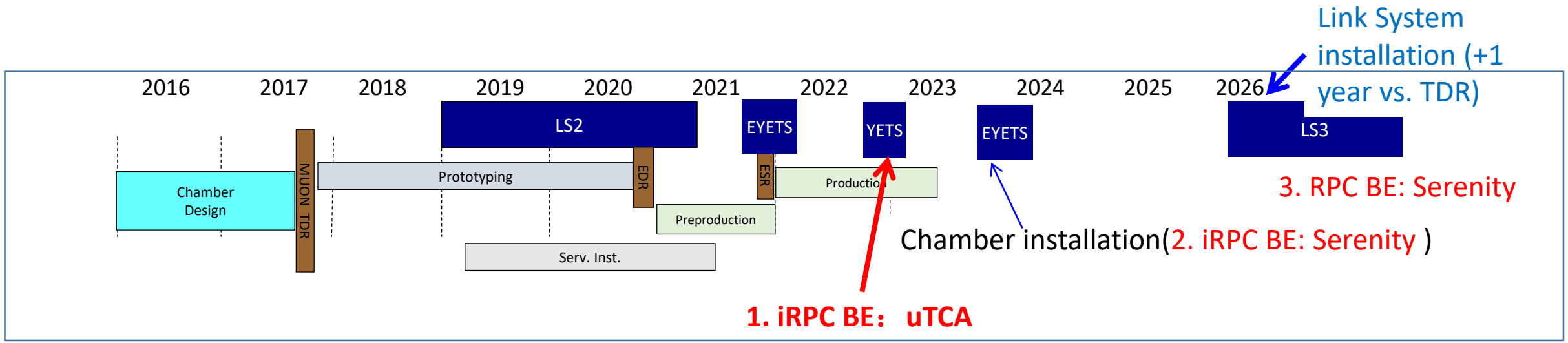
- Electronics

Dimensions: 165 cm x (63-114) cm

  - Each iRPC chamber is equipped with 2 **Frontend Electronics Boards (FEBs),** connected to **the backend electronics board (BEB)** via 2 GBT links.
    - The GBTx is a radiation tolerant chip that can be used to implement multipurpose high speed (3.2-4.48 Gbps user bandwidth) bidirectional optical links for high-energy physics experiments.
- iRPC spatial resolution (θ direction)
  - Hit position: r is calculated by the time difference of signals from two ends.
  - Much improved hit localization along the strip can be achieved. ~2 cm from cosmic test result.

BE Roadmap and Schedule agreed in RPC

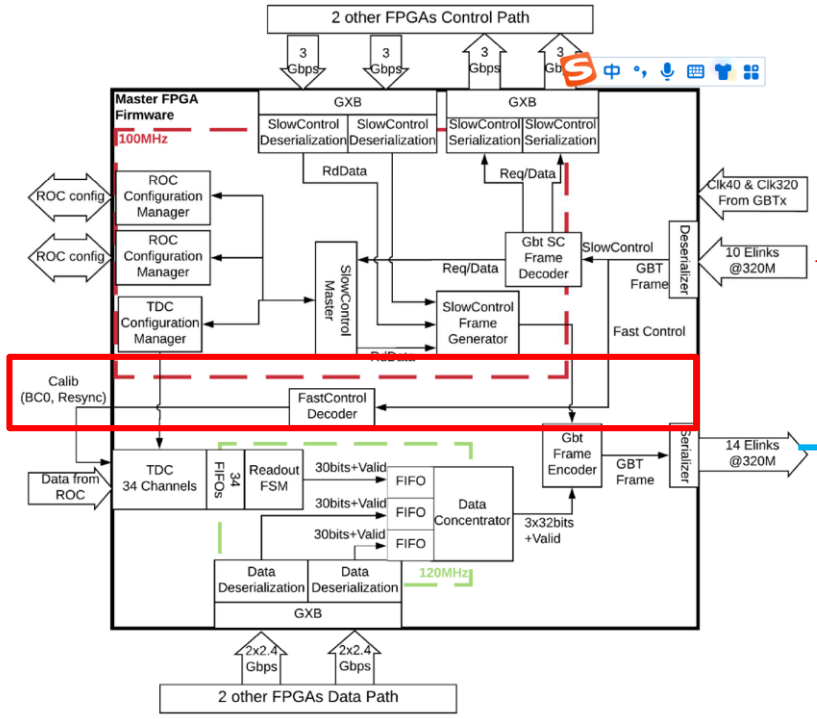
- **iRPC backend**
  - 2 Steps Installation Roadmap: uTCA+ATCA
  - **2022-2023: iRPC BE uTCA (current work for demonstrator)**
  - 2024: iRPC BE ATCA-Serenity (final system)



FEB signal timing

- FEB TDC timing principle

Focus on the central FPGA



BC0

BC0 feedback

BEB

- Fast control signal (BC0, Resync, etc.)
  - BC0—the first bunch among **3564** bunch crossing as time reference for FEB.
    - 3564 : circumference (26659 m)/bunch distance(7.48 m)
  - Received from backend on all FEBs within a fixed latency.

Slow Control Request Frame	Frame Header (Fast control)					Slow Control Request Information				Slow Control Payload	
Fied Name	Resync	BC0	ResetSCPath	MiscCtrl	FPGASel	RSVD	WrReq	BurstAdditionnalWords	Address	WrData0	WrData1
Field length	1	1	1	10	3	7	1	8	16	16	16
GBT Frame Group	G4					G3			G2	G1	G0

Slow Control Payload Frame	Frame Header (Fast control)					Slow Control Payload			
Fied Name	Resync	BC0	ResetSCPath	MiscCtrl	FPGASel	WrData(N)	WrData(N+1)	WrData(N+2)	WrData(N+3)
Field length	1	1	1	10	3	16	16	16	16
GBT Frame Group	G4					G3	G2	G1	G0

Slow Control Request Frame	Frame Header (Fast control)				
Fied Name	Resync	BC0	ResetSCPath	MiscCtrl	FPGASel
Field length	1	1	1	10	3
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Slow Control Payload Frame	Frame Header (Fast control)				
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Field length	1	1	1	10	3
GBT Frame Group	G4				

System timing from backend

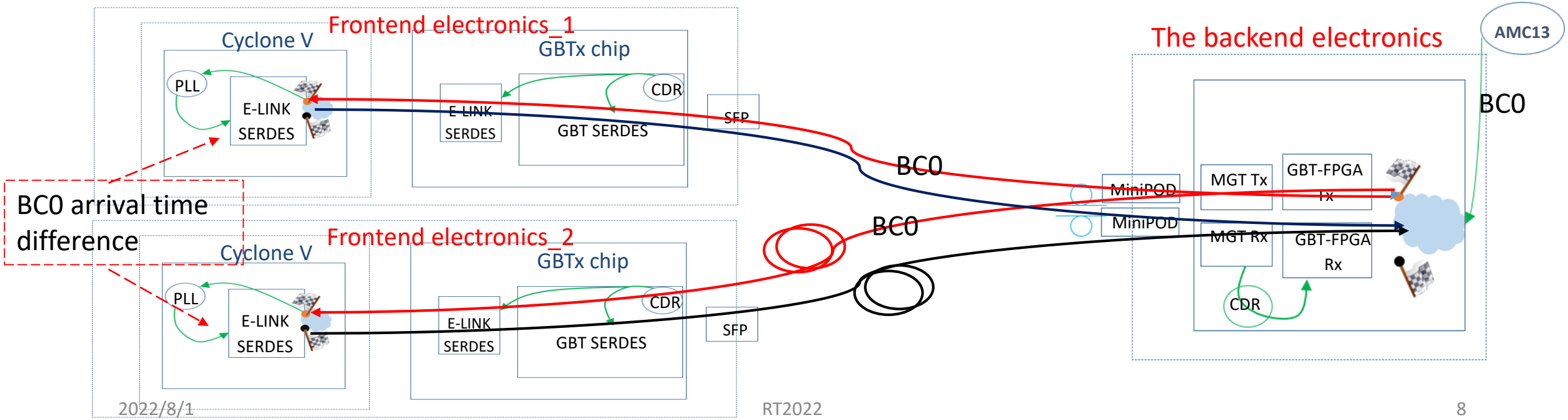
- Functionalities/tasks of iRPC Backend
  - Slow Control (powering up FEB, TDC configuration, Petiroc configuration…)
  - Monitoring
  - Fast Control (BC0 distribution …)
  - Trigger primitive (Clusterzation)
  - Readout (DAQ)

- Difficulties
  - How to develop and verify BEB functions in lab without test facility like detector, FEB, or GBTx chip ?
  - What is the clock requirement of FEE and how to realize?
  - How to synchronize different links in the backend ?

- iRPC FEB emulator study.
- Timing reference distribution and correction of distribution difference .

Timing reference distribution

- Problem
  - The Bunch Cross 0 (BC0) signal from AMC13 as a timing reference is distributed to each FEB located in different RPC stations by BEB.
    - AMC13: This module is designed to provide TTC, DAQ and TTS services to modules in a MicroTCA crate for CMS.
  - Arrival times of BC0 between links are different.
    - Latency = T_GBT FPGA + T_length + T_GBTx , T_GBT FPGA and T_GBTx are the same for all FEBs.
    - **Different fiber lengths lead to different latencies** and this need to be measured and corrected.

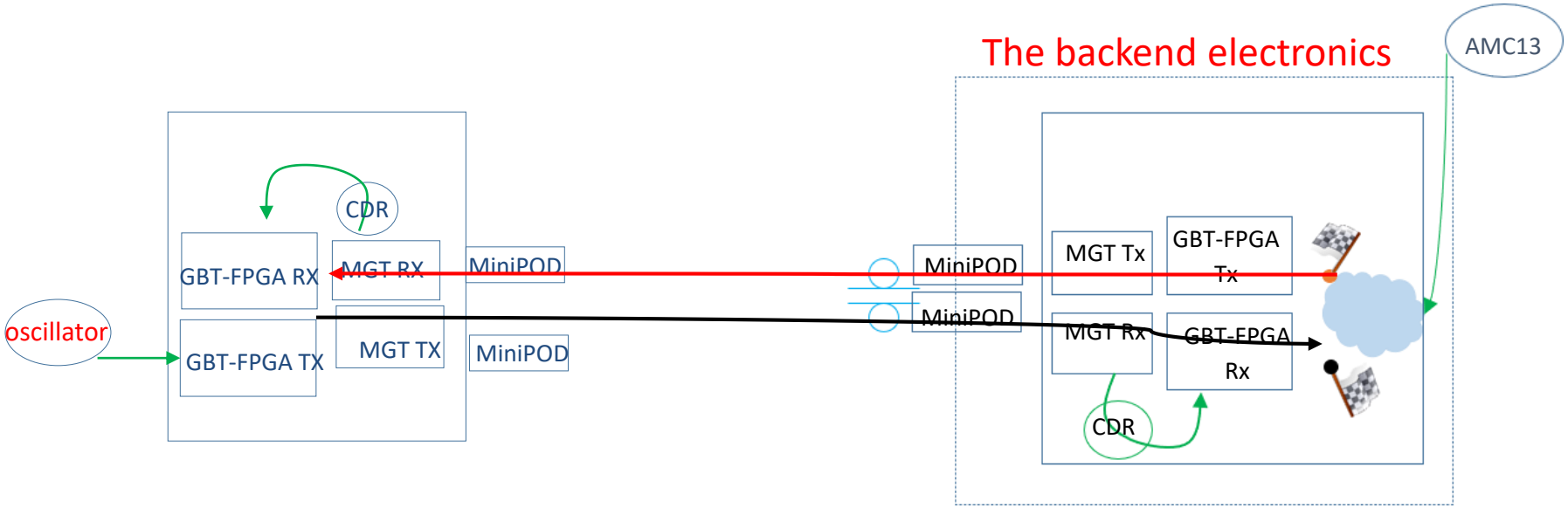


Correction of distribution difference

- Solution
  - Latency measurement need to be done.
    - latency must be fixed values and measured accurately.
  - A 12-bit counter of the 2.5 ns step is developed in BEB and used to measure the loopback time of different links. through a self-defined handshake mechanism.
    - The downlink and uplink are estimated to have same time consuming and the difference is caused by different fiber length.
    - Taking the faster link as the reference we apply a correction value to the slower link according to the loopback time via slow control.
    - Correction value (1.25 ns step) = (Latency_big - Latency_small)/2 .
    - TDC data on each FEB will minus its specific correction value to minimize the latency difference between paths.

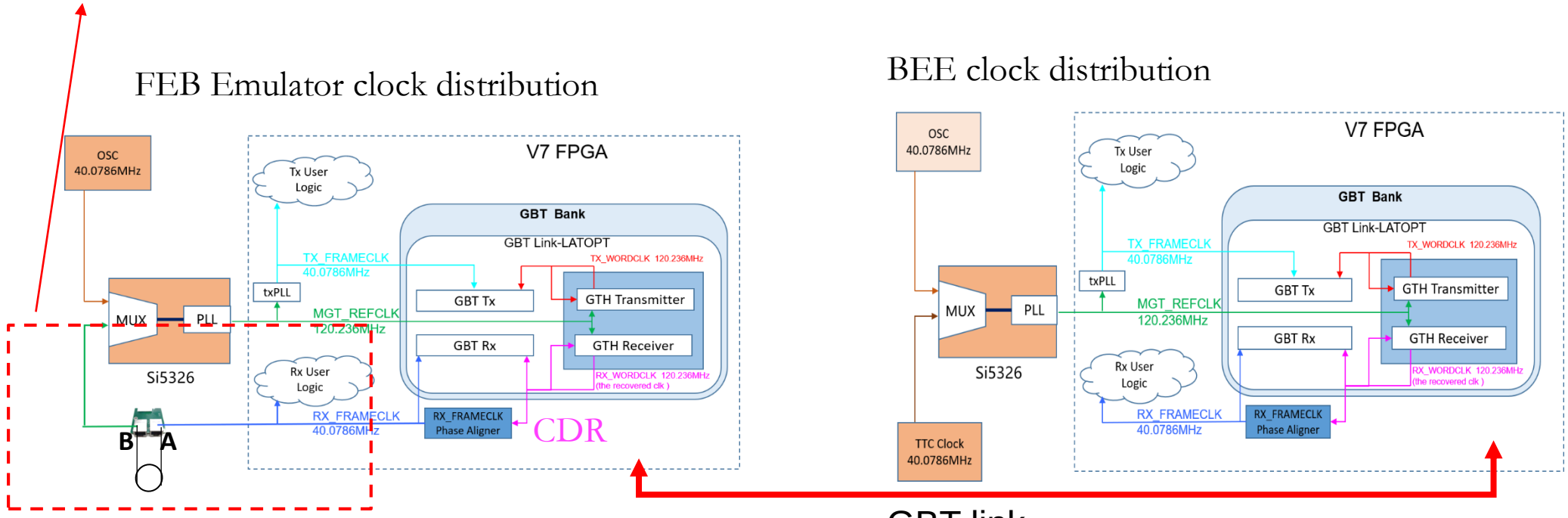
Implementation in FEB emulator

- Before we have the real FEB electronics, we did the test using GBT-FPGA based emulator.
- FEB emulator Rx CDR clock is synchronous with BEB system clock.
- Managed to use Rx CDR clock as GBT-FPGA Tx clock.
  - Through RJ-45 daughter board.



System clock generation in FEB emulator

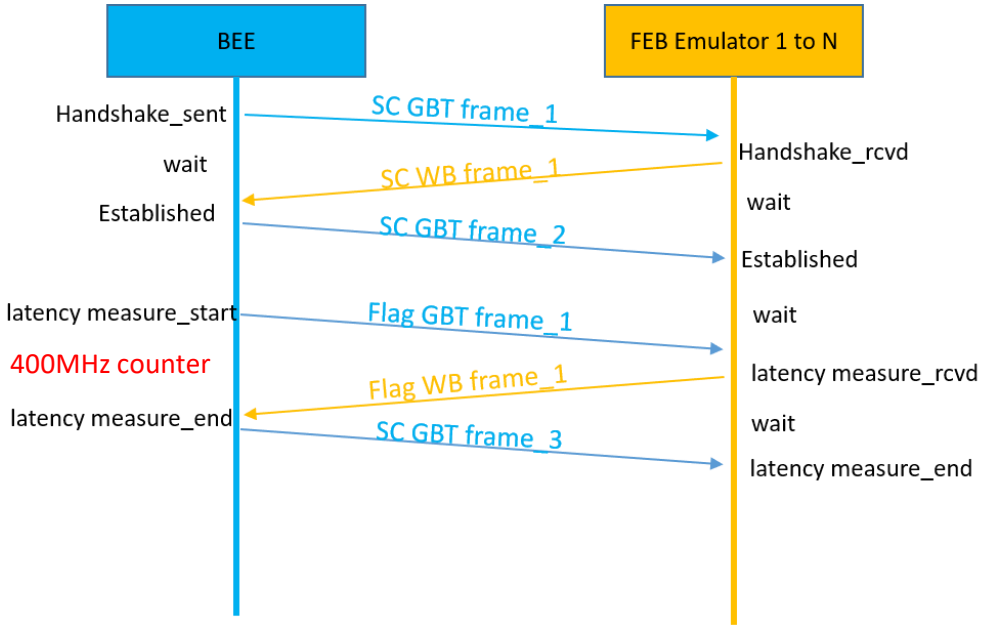
- The backend -- 40.0786MHz system clock from AMC13 .
- FEB emulator –40.0786MHz OSC after power up.
- Rx CDR clock is generated and aligned on FEB emulator.
- **Then Rx CDR clock is fanned out through RJ45 A and connected to RJ45 B .**
- **Clock from RJ45 B replaces OSC as FEB emulator system clock after MUX.**



synchronous with system clock

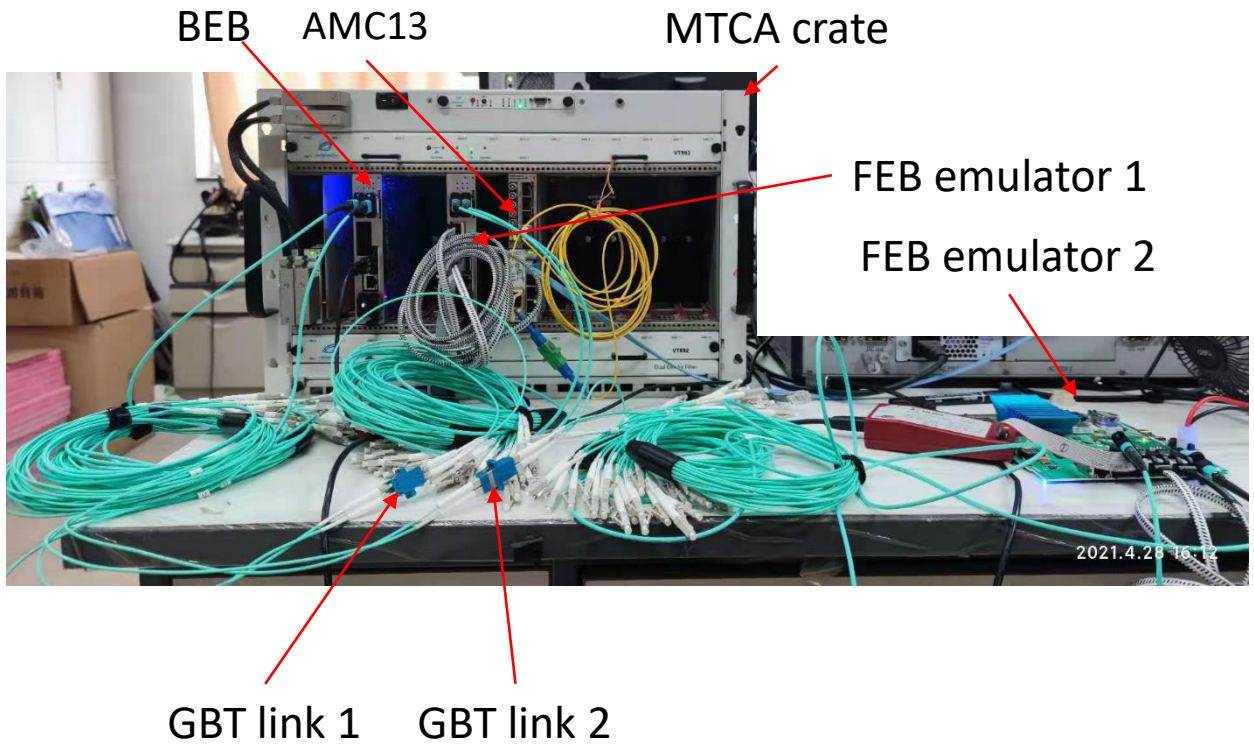
Correction implementation

- Latency measurement



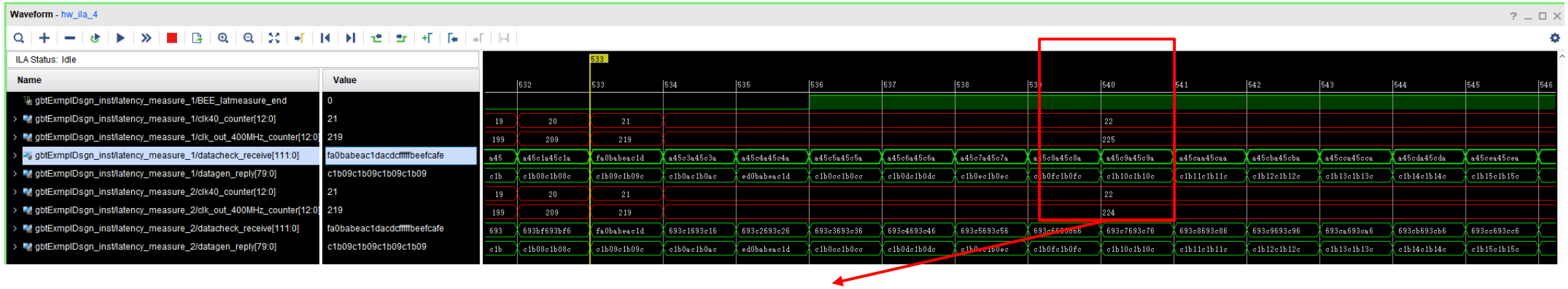
measurement mechanism

- Test System setup in Beijing lab
  - System clock source: AMC13
  - Backend : 1 BEB
  - Frontend :2 FEB emulators(represent the 2 FEBs on 1 iRPC chamber)



test result

- Latency measurement Test result



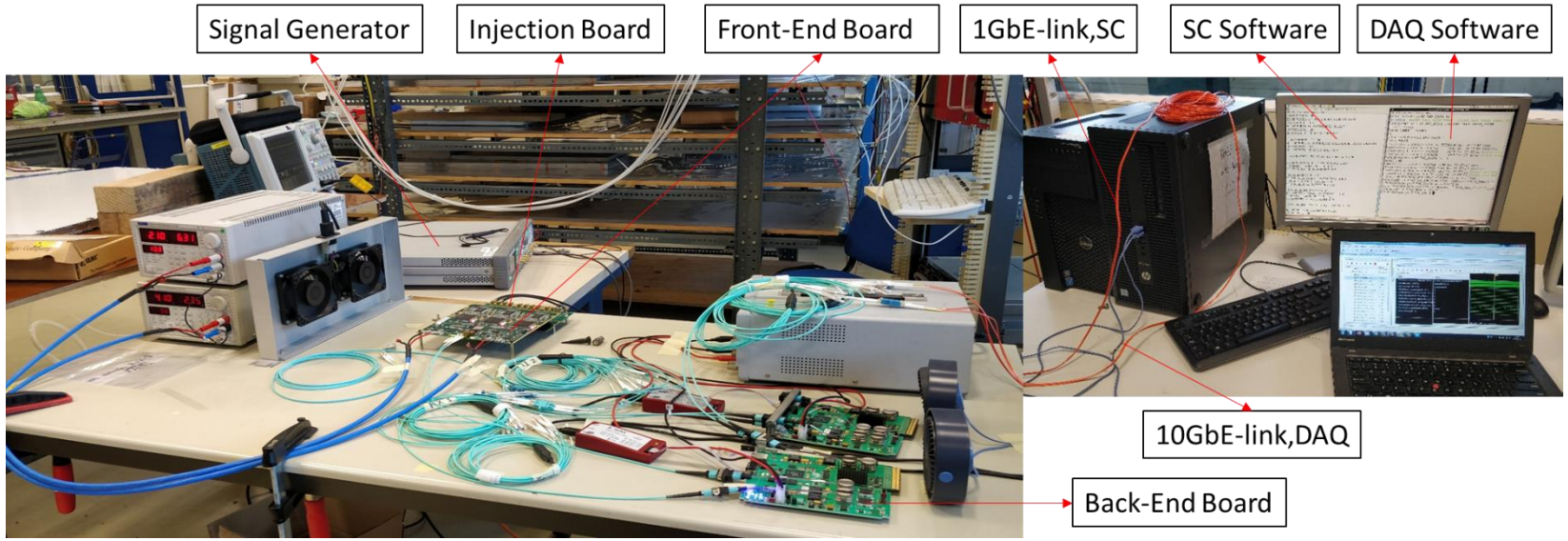
Measurement time step	25ns --BX clock	2.5 ns --coarse time
BEB to FEB emulator1 cnt	22*25 = 550 ns	216 * 2.5 = 540.0 ns
BEB to FEB emulator2 cnt	22*25 = 550 ns	215 * 2.5 = 537.5 ns

Δ = 2.5 ns

A deterministic latency between BEB and FEB emulator was achieved and measured, indicating that the test system works normally.

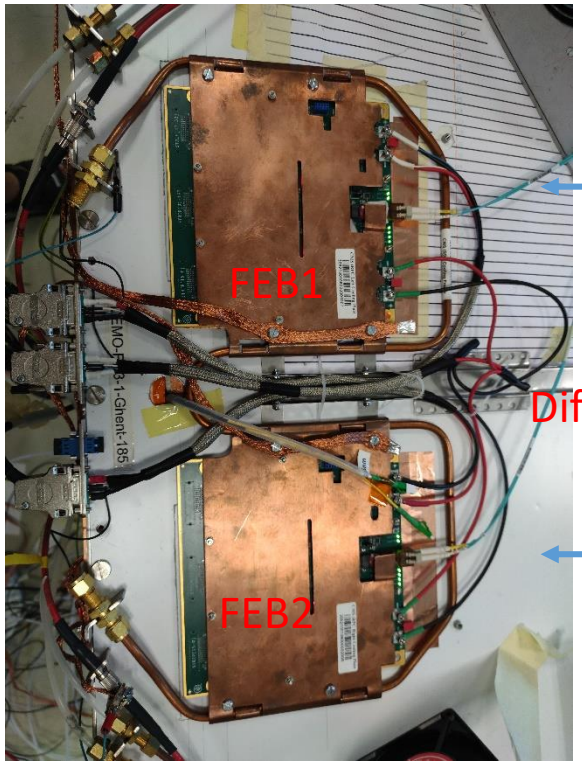
BEB to one FEB joint test

- Joint test system setup
  - One backend board receives 1 link from FEB.
  - The backend performs slow control (FEB powering up, configuration, etc.) and fast control (BC0 distribution, etc.) for the FEBs.
- Test results
  - When the FEB receives a BC0, it will sent the BC0 timestamp to backend. The result shows that the backend sends BC0 to FEB every 3564BX constantly, indicating the system works normally.
  - The sigma of BC0 timestamp from FEB is 23.32 ps proves that the distribution of BC0 is successful.

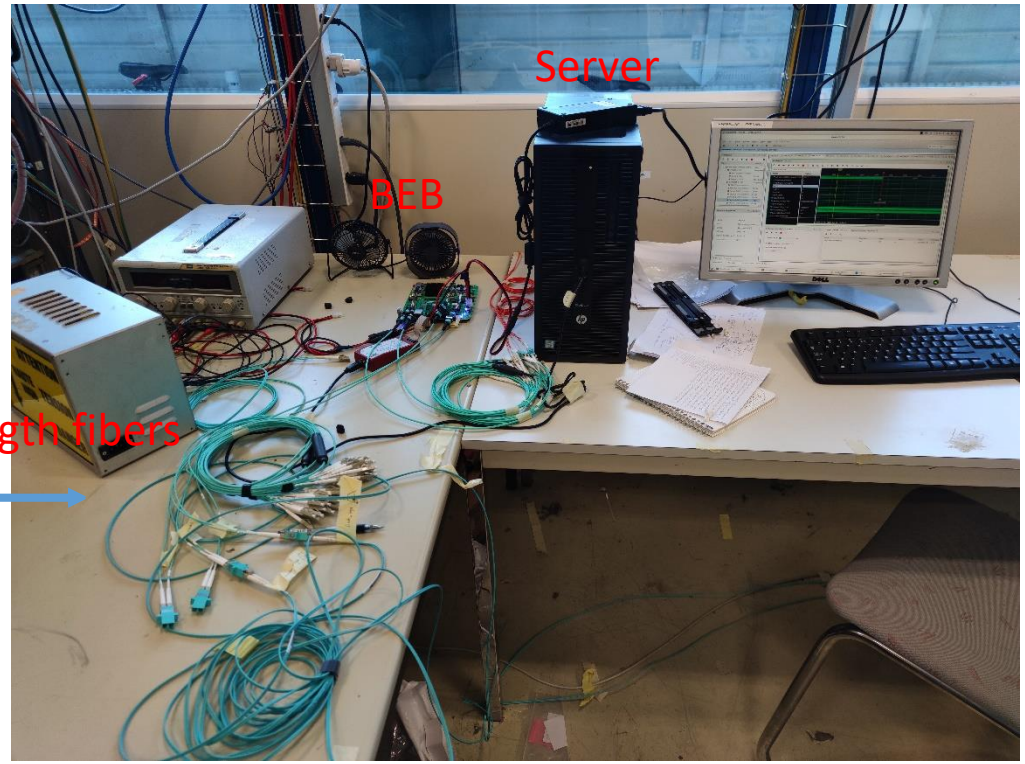


BEB to two FEB joint test

- Joint test system setup
  - One backend board receives 2 links from FEBs.
  - The length of fibers are different to simulate real cases.

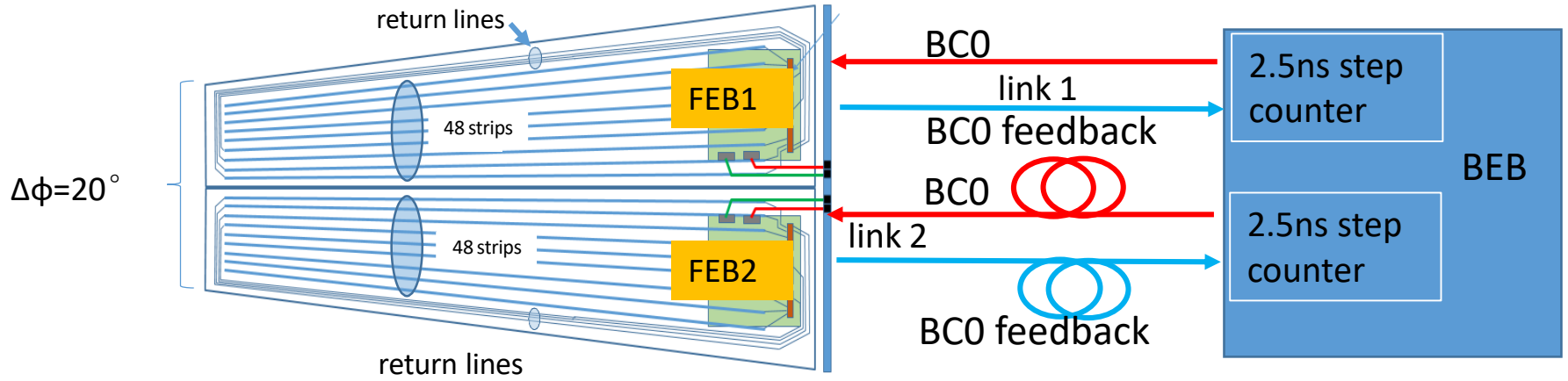


Different length fibers



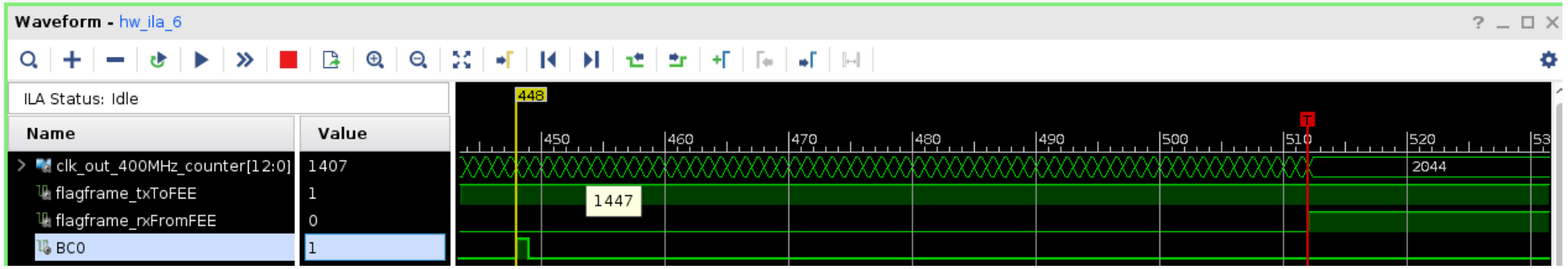
BEB to two FEB test method

- Detail
  - The BC0 distribution to one FEB has been proved successful.
  - This method was used to measure the latency between two links, **which will affect the backend trigger function rather than iRPC position resolution.**
    - Eg. If muons hit the middle of the chamber, FEB1 and FEB2 will give same position(~2 cm) but different timing because of different latency.
  - The backend records the start of BC0 distribution and the end of BC0 feedback via a 12-bit counter of the 2.5 ns step.
  - Half of the the time difference(1.25 ns step) between two links will be used to correct the slower link via slow control.

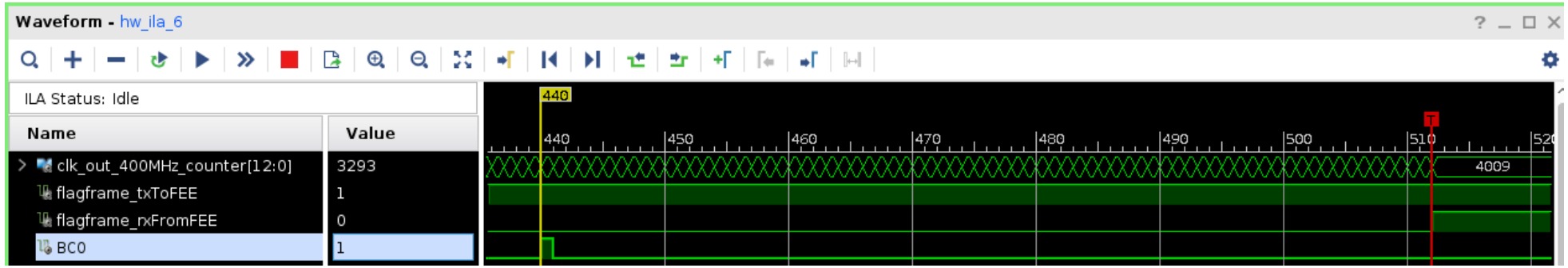


BEB to two FEB quick test result

- Latency measurement test result



Latency_FEB1 = 2044-1407=637 (2.5 ns)



Latency_FEB2 = 4009-3293=716 (2.5 ns)

Correction value = (716-637)/2 = 39.0

A deterministic latency between BEB and FEB was achieved and measured, this latency difference can be used to correct the FEB TDC timestamp.

Next step

- The latency measurement requirement (2.5 ns/1.25 ns/smaller?) and effect need to be studied further.
- The implementation of latency measurement can be improved based on requirement.

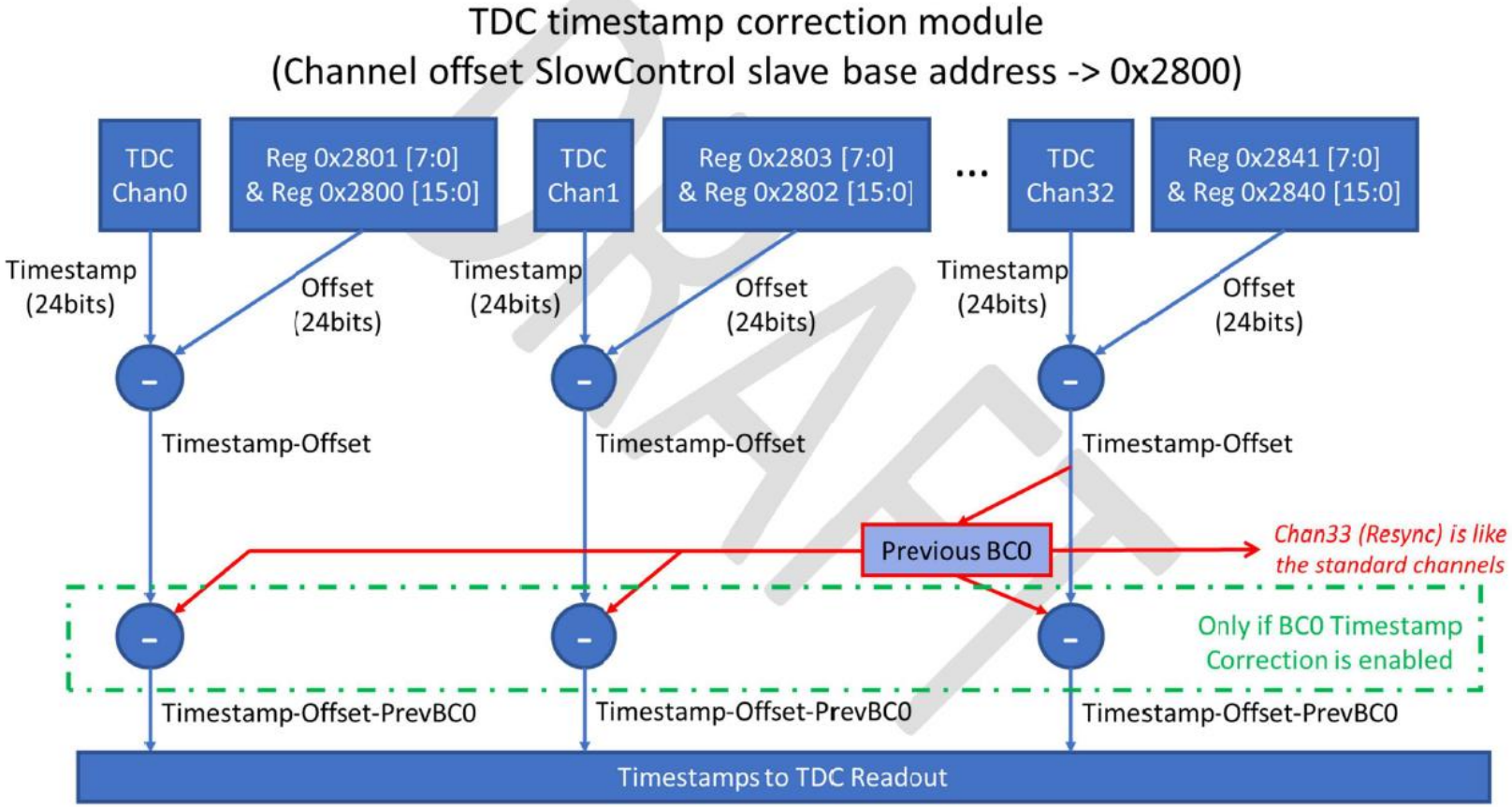
Summary

- iRPC timing reference issue including FEB signal timing and backend system timing has been researched and verified.
- Timing reference distribution and correction has been studied in both emulator and FEB.
- The test results show that the sigma of BC0 distribution is 23.32 ps which will be used for iRPC position calculating. The latency between two links was measured and waiting to be corrected and verified in the next step.

Thanks!

Backup

FEB TDC timestamp correction module



Rx CDR clock introduction

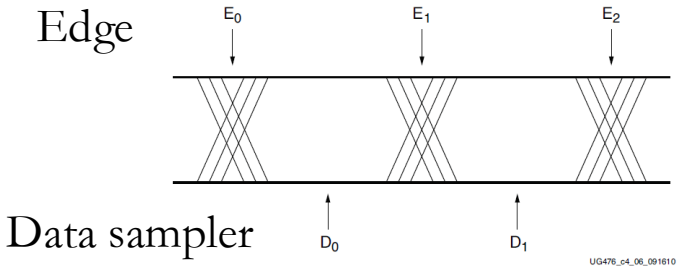


Figure 4-22: **CDR Sampler Positions**

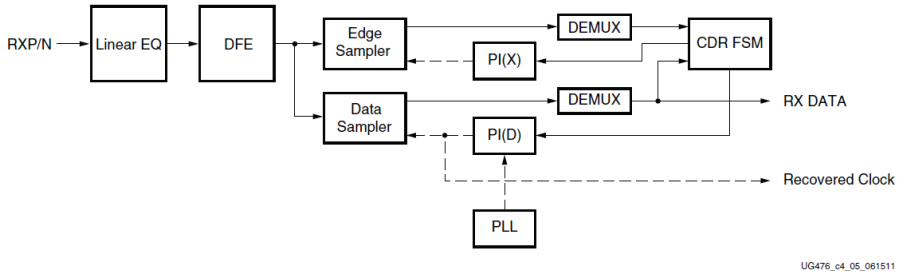
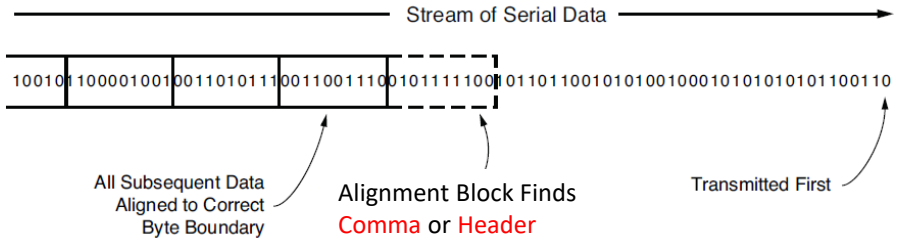
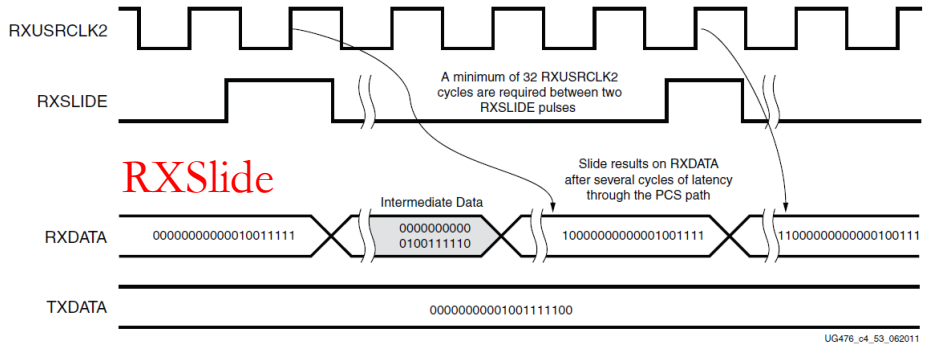


Figure 4-21: **CDR Detail**

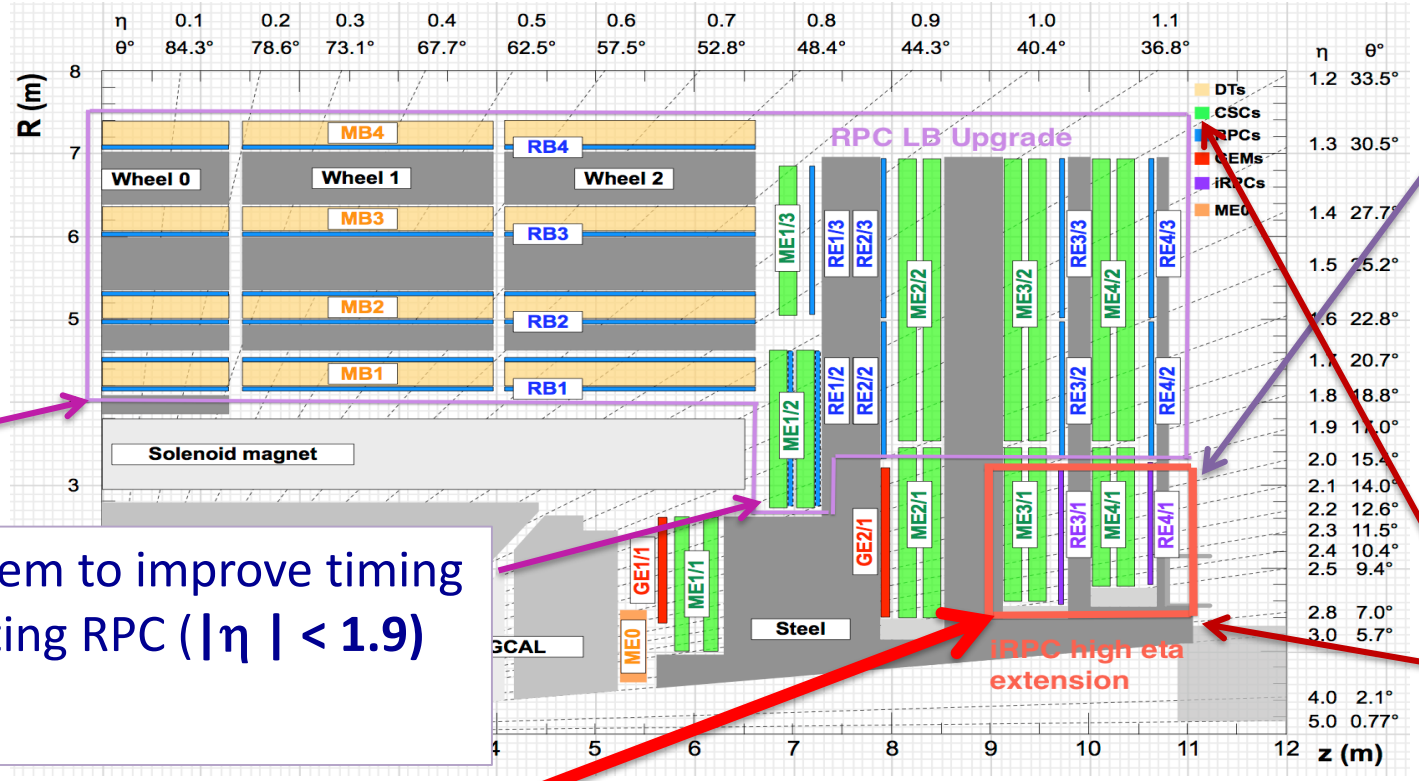




- The CDR state machine uses the data from both the edge and data samplers to determine the phase of the incoming data stream and to control the phase interpolators (PIs)

The data is shifted right by one bit for every RXSLIDE pulse issued. The GBT receiver searches for the Header in the incoming data and checks it. Link is established after GBT Rx receiving 24 successive Headers(0110/0101). Then use Header flag to align the Rx CDR clock.

Phase 2 RPC Upgrade Project Overview



Upgrade of Link System to improve timing resolution for existing RPC (**|η| < 1.9**)

Certification for HL_LHC

Back-End for present and new high eta region RPCs

Extend the RPC coverage up to |η| = 2.4 to increase redundancy in high eta region in stations 3 and 4