

General Backgrounds of NICA-MPD ECAL

❑ NICA Multi Purpose Detector (MPD)

- A 4π spectrometer for heavy-ion collision detection at high luminosity
- Au+Au interactions at 6 kHz, with multiplicity: >1000 charged particles for central collisions at $\sqrt{s_{NN}} = 11 \text{ GeV}$

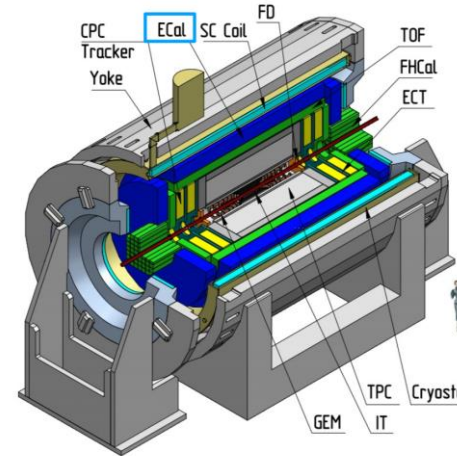
❑ The previous FEE for Electromagnetic Calorimeter (ECal)

- **Shashlik-type calorimeter:** bremsstrahlung photons collected through optical wavelength shifter (WLS) fibers, coupled with SiPM detectors
- **FEE:** SiPM readout board (shaping and anti-alias filter), together with a 64-channel 14-bit, 62.5 MS/s commercial ADC board

- **Performance:** $\sigma_t \sim 1 \text{ ns}$, $\frac{\Delta E}{E} = 6\%$

❑ Timing requirement

- $\sim 10 \text{ ns}$: background and pile-up cancellation to zero
- $\sim 1 \text{ ns}$: suppress secondary background events down to negligible level
- Sub-ns: work in the ToF mode for auxiliary time measurements
 - ECal TDR: reach the level of 150 ps



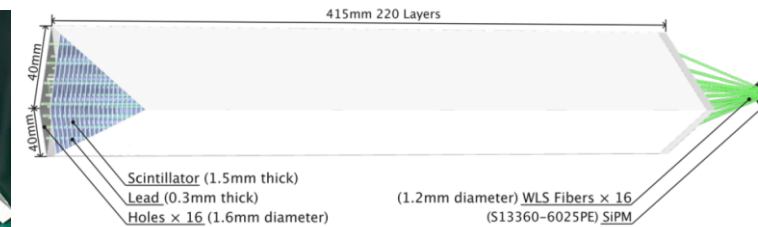
General layout of MPD (central part)

1st stage

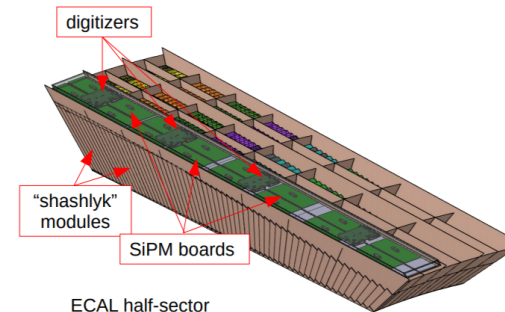
- SC Coil – superconducting solenoid
- IT – inner tracker
- TPC – time-projection chamber
- TOF – time-of-flight system
- ECal – electromagnetic calorimeter
- FD – fast forward detectors
- FHCAL – forward hadron calorimeter

2nd stage

- ECT – endcap tracker
- CPC – cathode pad chambers



1/6 of the half-sector of the ECal (Zone 8) and single tower structure (Cited from: Y. Li et al 2022 JINST 17 T04005)



- 38,400 readout channels
- 14 bit, 62.5 MS/s digitizers
- 600 digitizer boards inside MPD magnet
- 38 data merger boards in electronics racks
- 10 kW dissipated power

ECAL half-sector

* drawing shown for illustrative purposes only

Welcome to Poster #36

@ Poster B Section !!

Introduction and motivation

Readout Design Architecture

Pre-amp a RF transistor current follower with a differential op-amp

ADC 12bit 200MS/s pipeline SAR ADC

SPICE simulation for pre-amp in working scenario

A fast front-end readout design for NICA-MPD shashlik electromagnetic calorimeter

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INTRODUCTION

- Electromagnetic Calorimeter (ECal)**
 - Shashlik sampling structure
 - Bremsstrahlung photons collected through optical wavelength shifter (WLS) fibers
 - Coupled with Silicon photomultipliers (SiPMs) readout
- SiPM Readout**
 - Large terminal capacitance detector (~100 pF)
 - Nonlinear behavior arises with a finite input impedance amplifier
 - Readout structure: trans-impedance (TIA) or common-base amplifier
 - Undesired effects: gain peaking and ringing of the output

PRELIMINARY TEST

- Laser test for preamplifier**
 - Signal rise time ~1.4 ns, giving the estimation of an expected bandwidth of roughly 250 MHz
 - Single-channel time resolution performance better than 20 ps (sampling rate @10GS/s)
- Chip test for ADC**
 - Maximum sampling rate ~160MHz
 - Input a sine wave with a frequency of 80 MHz and an amplitude of -1dBFS, the effective number of bits (ENOB) is 9.34, the spurious-free dynamic range (SFDR) is 73.8 dBc

READOUT DESIGN

- Preamplifier**
 - Detector: Hamamatsu multi-gigapixel photon counter (MPPC) S13360-6025 (typ. 1280 pF/ch)
 - Circuit: a RF transistor current follower with a differential op-amp
 - Working scenario: with an incident of 2000 photons, the output is ~750 mV (V_{com}), ~1.5 V (V_{diff})
 - PCB: 16 channels offers dual outputs
- ADC**
 - 12bit 200MS/s pipeline SAR ADC architecture
 - Two-step conversion process (6+7 bits), DAC1 with a smaller capacitance (64f) while the MDAC DAC (1.4pF)
 - A redundancy design is employed to effectively mitigate the V_{ref} buffer requirements

SYSTEM PERFORMANCE TESTING (PROOF OF CONCEPT)

- Electrical test**
 - Preliminary system-level time response assessments were performed using an established 14-bit 1 GHz acquisition card (called WRX0608A1, V_{pp}=1.6 V)
 - Preamplifier configuration was changed for different output rise time test
 - A square wave signal was generated by an arbitrary function generator (Tektronix AFG3102C)
 - Data processing includes sparse sampling, with an equivalent sampling rate of 200 MHz
 - Waveforms with 3~4 sampling points (rise time at 15~20 ns for 200 MHz sampling rate) on the rising edge has better time resolution ~20 ps (@output ≥250mV)

SPICE SIMULATION

- Preamplifier SPICE results**
 - Software: LTSpice XVII
 - SiPM Model:

Hamamatsu S13360-6025 Parameters						
G (10 ⁵)	N _{cells}	C _d (fF)	C _g (pF)	R _q (kΩ)	C _q (fF)	V _{bias} (V) M (ph)
7.13	57600	20.84	41.1	794	1.6	-56.9 2000

- Preamplifier SPICE results:**

SUMMARY

- A fast front-end readout design was designed and developed. The prototype preamplifier and ADC chip performance were evaluated.
- Preliminary system time response assessments were performed. Verification had shown that good time resolution performance can still be achieved at low sampling rates (200MHz).

Preliminary Test Results

- Pre-amp:** BW~250 MHz
 - Single-channel time resolution better than 20 ps
- ADC:** ~160 MS/s (max.)
 - ENOB=9.34 bit, SFDR=73.8 dBc

System Performance

- PROOF OF CONCEPT**
 - For 200MS/s sampling rate: proper configuration (3~4 sampling points on the rising edge) can achieve time resolution ~20 ps (@output ≥250mV)