The Design of an 8-channel, 41.7-ps Resolution Time-to-Digital Converter for STCF ECAL

24th IEEE REAL TIME CONFERENCE
Quy Nhon, Vietnam
April 22-26, 2024

Ziwei Zhao[1], Ran Zheng[1*], Jiale Li[1], Jia Wang[1], Xiaomin Wei[1] , Ruiguang Zhao[1] , Feifei Xue[1] and Yann Hu[1]

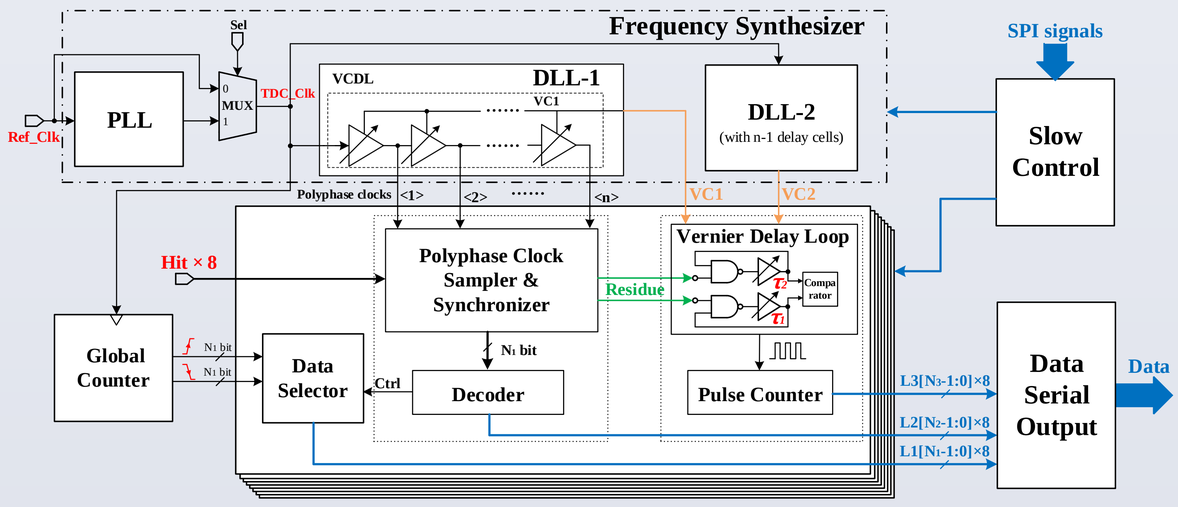
1. School of Computer Science and Engineering, Northwestern Polytechnical University, Xi'an, China

Author: Ziwei Zhao

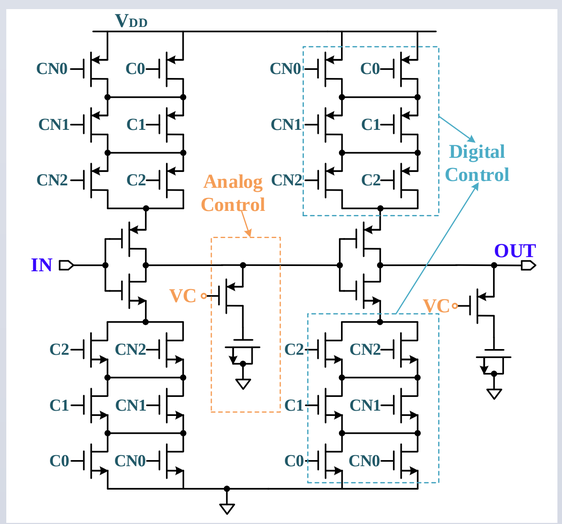
Introduction

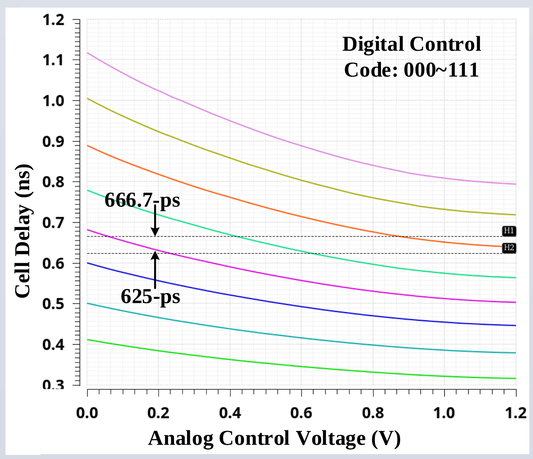
- High time resolution (100-ps) is required in the electromagnetic calorimeter (ECAL) of the Super Tau-Charm Facility (STCF), for background suppression, gamma-neutron discrimination and events identification.
- The Pure CsI (pCsI) crystal scintillator with an avalanche photodiode (APD) readout is adopted in STCF EMC and time stamps are acquired through front-end readout circuit (ROC) and digitized with TDC.
- An 8-channel vernier delay loop (VDL) based TDC ASIC is proposed in this paper. With 3-level quantization and 100-MHz reference clock, the TDC can get a dynamic range of 2.56-μs and resolution of 41.7-ps.

The Design of TDC

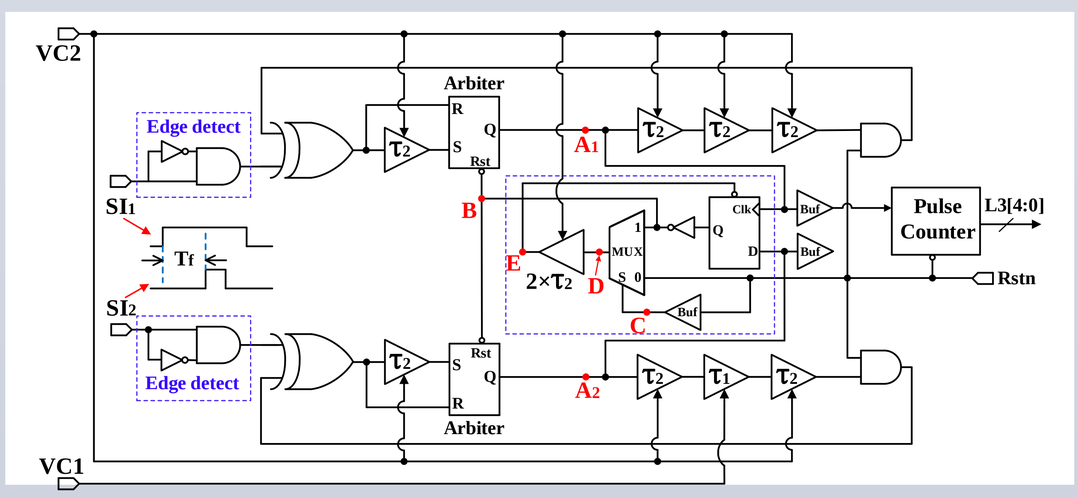


- The 1st level: A global dual-edge triggered counter with metastability immunity, shared by 8 TDC channels. (8-bit, LSB_1 = 10 ns)
- The 2nd level: poly-phase interpolators. (4-bit, LSB_2 = 625 ps)
- The 3rd level: vernier delay loop implemented with two DLLs. (5-bit, LSB_3 = 41.7 ps)



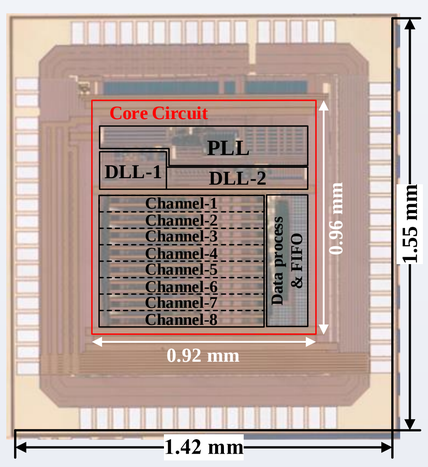


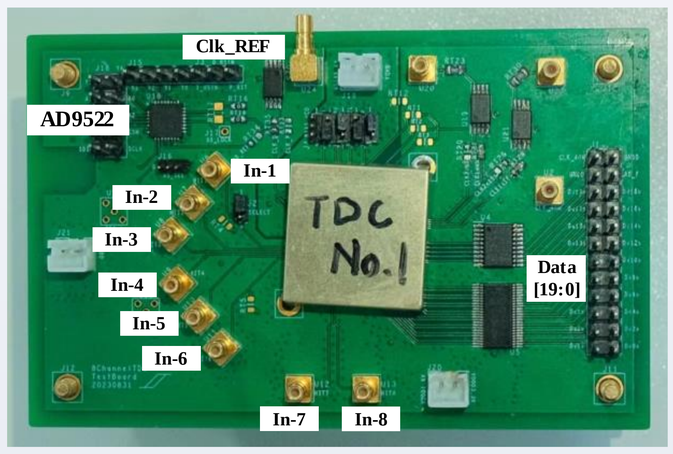
A Novel Delay Cell for low-jitter DLL and VDL:
Serial Current Starve (Digital) + Shunt capacitor (Analog)

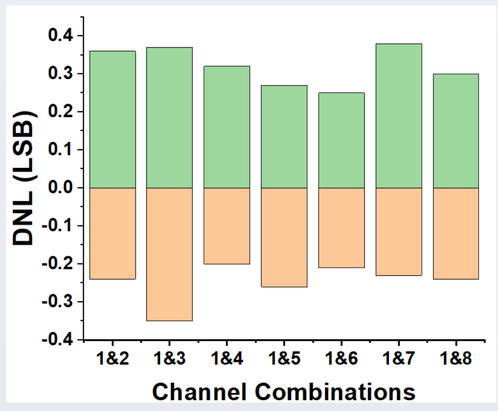


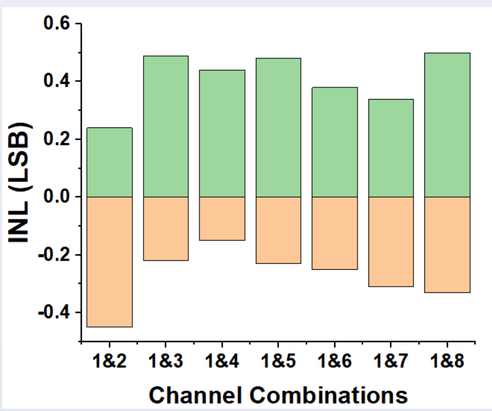
VDL with Automatic Reset Mechanism

ASIC Prototype & Test Results

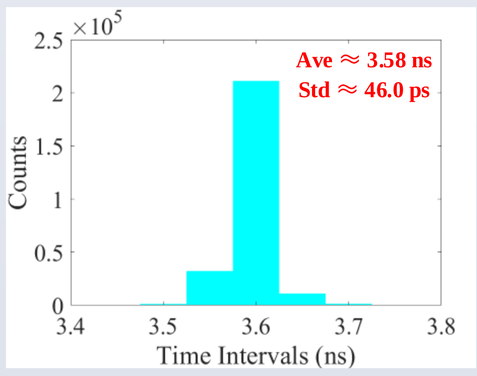




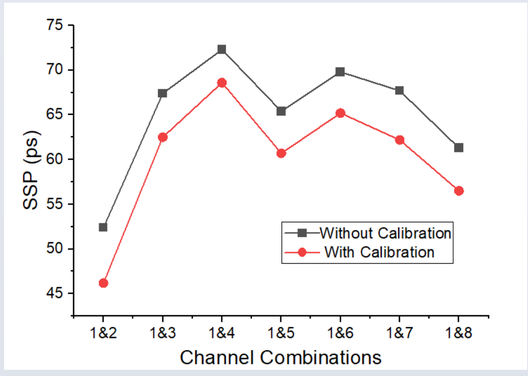




- Asynchronous TDC test (with dual channels): the sliding scaled technique makes linearity better!



- SSP with channel 1&2 (best)



- SSP with all channel combinations

Calibration: $TDC_{CAL} = TDC_{RAW} + INL[TDC_{RAW}]$

Conclusion & Comparison

Parameters	[1]	[2]	[3]	[4]	[5]	This work
Process (nm)	130	350	65	110	180	180
Type	Delay line	GRO*	Vernier	Counter	VCRO*	Vernier
Channels	1024	48	2	17	1024	8
Dynamic range (ns)	100	51.8	2500	3400	2100	2560
SSP (ps)	78.5	93.2	27.6	104	62.1	46.0
DNL/INL (LSB)	0.4/1.2	2.0/2.4	1.7/2.8	0.3/2.5	0.5/2.2	0.4/0.5
Conversion Rate (MS/s)	500	40	1	/	/	22.2
Power (mW)**	90	/	51.4	188.8	>1200	93.6***

* GRO is the acronym of Gated Ring Oscillator and VCRO represents Voltage Controlled Ring Oscillator.
** The power consumptions of all TDC channels are included.
*** The presented power dissipation of proposed chip is obtained with the conversion rate of 4-MS/s.

- An 8-channel, high precision TDC ASIC has been designed.
- The TDC features with a single-shoot precision of 46-ps for the best case, the DNL and INL both better than 0.5-LSB and good consistency among all channels.

REFERENCE

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西北工业大学 NORTHWESTERN POLYTECHNICAL UNIVERSITY

Contact: zhaozw@mail.nwpu.edu.cn
zhengran@nwpu.edu.cn (Corresponding author)