Development of the Low Noise Front-end Electronics for Pulse Voltage Stability Measurement

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Motivation

In order to achieve the stability measurement of 10V high-voltage pulses on an oscilloscope, this paper designs a low-noise front-end electronics to adjust the high-voltage pulse bias to near 0 V, and then uses the oscilloscope to perform measurements at a resolution of 1 mV/div.

Design of Low Noise Front-end Electronics

➢ Modulator Specification

Description	Result
Output Voltage	-160 kV
Output Current	116 A
Voltage Rise Time (10%-90%)	$\leq 1\ \mu s$
Voltage Fall Time (90%-10%)	$\leq 1\ \mu s$
Pulse Half Width	$5.5\ \mu s$
Flat Top Ripple or Droop	$\leq \pm 1\%$
Voltage Pulse to Pulse Stability	$\leq 50\ ppm\ (rms)$
Pulse Leading Edge Jitter	$\leq 10\ ns\ (rms)$
Repetition Rate	$\leq 250\ Hz$

➢ Low Noise Front-end Electronics

- ➢ provide a clean 10 V DC voltage
- ➢ make a difference with the input 10 V voltage pulse
- ➢ shift the flat top of the pulse of interest to near 0 V
- ➢ a discrete three-op-amp instrumentation amplifier

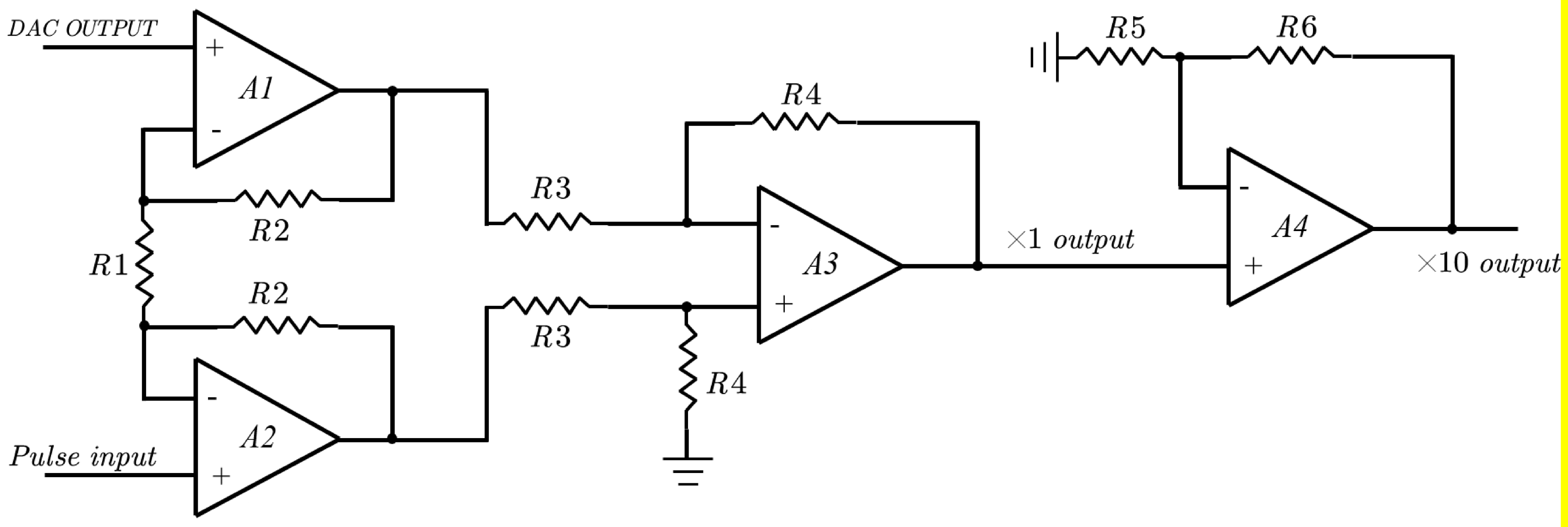


Fig. The low noise front-end electronics schematic based on discrete three op-amp instrumentation amplifier.

Circuit Analysis

The common mode rejection ratio (CMRR) of the discrete instrumentation amplifier

$$CMRR = \frac{G \times CMRR_3 \times CMRR_{12}}{G \times CMRR_3 + CMRR_{12}}$$

The CMRR of the first stage, where the CMRR1 and CMRR2 is the CMRR of amplifier A1 and A2, respectively.

$$CMRR_{12} = \frac{CMRR_1 \times CMRR_2}{CMRR_1 - CMRR_2}$$

➢ Improve CMRR

- ➢ the parametric matching of the first-stage op amp
- ➢ higher first-stage gain
- ➢ higher second-stage op amp CMRR
- ➢ second-stage precision matching resistor network

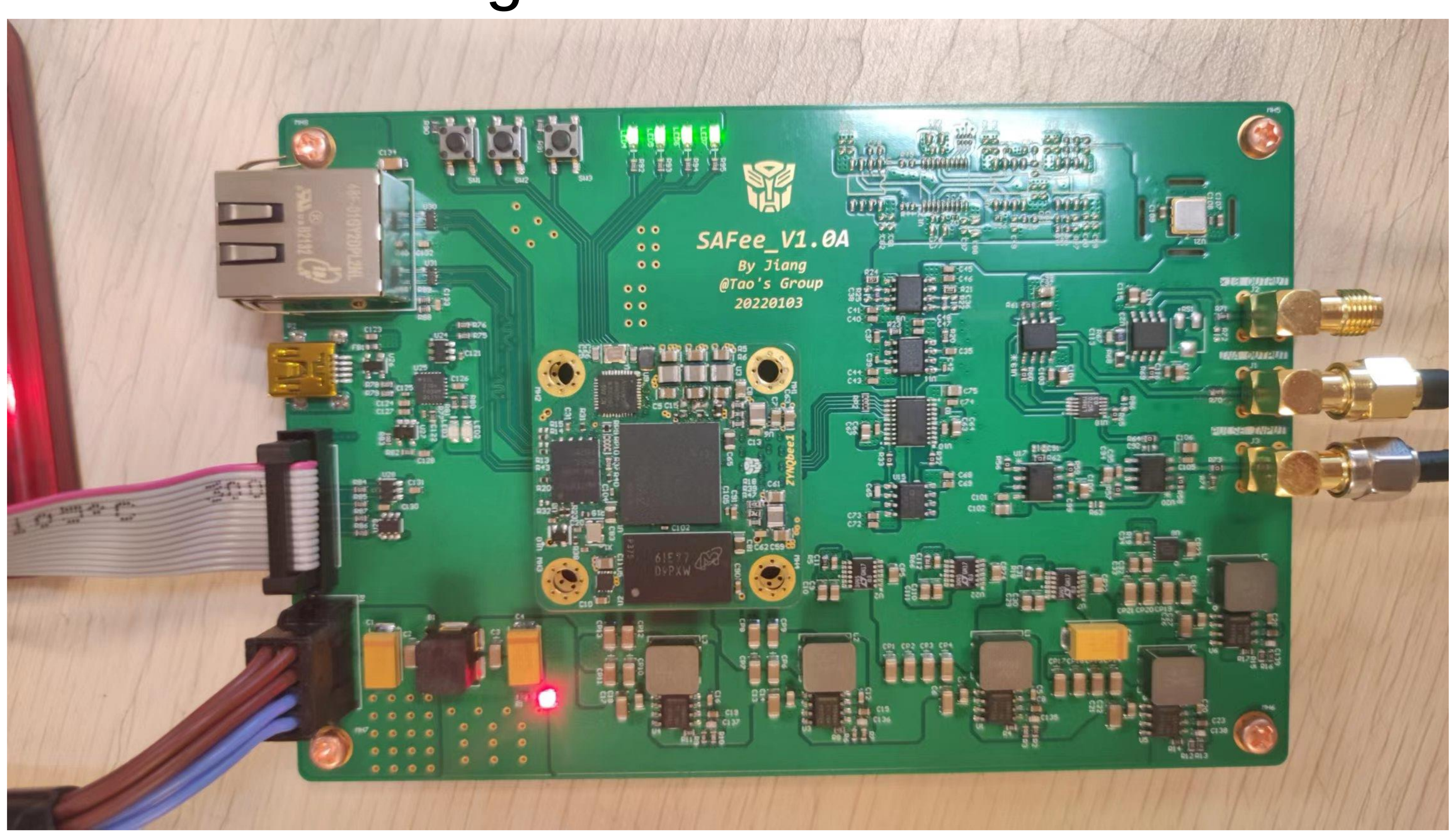
➢ Noise Reduction

- ➢ the output noise spectral density of A1 and A2
- ➢ the output noise spectral density of A3

$$V_{n1}(rms)^2 = {e_{n1}}^2 \cdot \left(1 + \frac{2 \cdot R_2}{R_1}\right)^2 + (i_{n1} \cdot R_2)^2 + {e_{nR2}}^2 + \left(\frac{e_{nR1}}{\sqrt{2}} \cdot \frac{R_2}{R_1}\right)^2$$

$$V_{n3}(rms)^2 = \left[e_{n3} \cdot \left(1 + \frac{R_4}{R_3}\right)\right]^2 + 2 \cdot (i_{n3} \cdot R_4)^2 + {e_{nR4}}^2 + \left(e_{nR3} \cdot \frac{R_4}{R_3}\right)^2 + \left[e_{nR34} \cdot \left(1 + \frac{R_4}{R_3}\right)\right]^2$$

Hardware Design and Test of SAFee

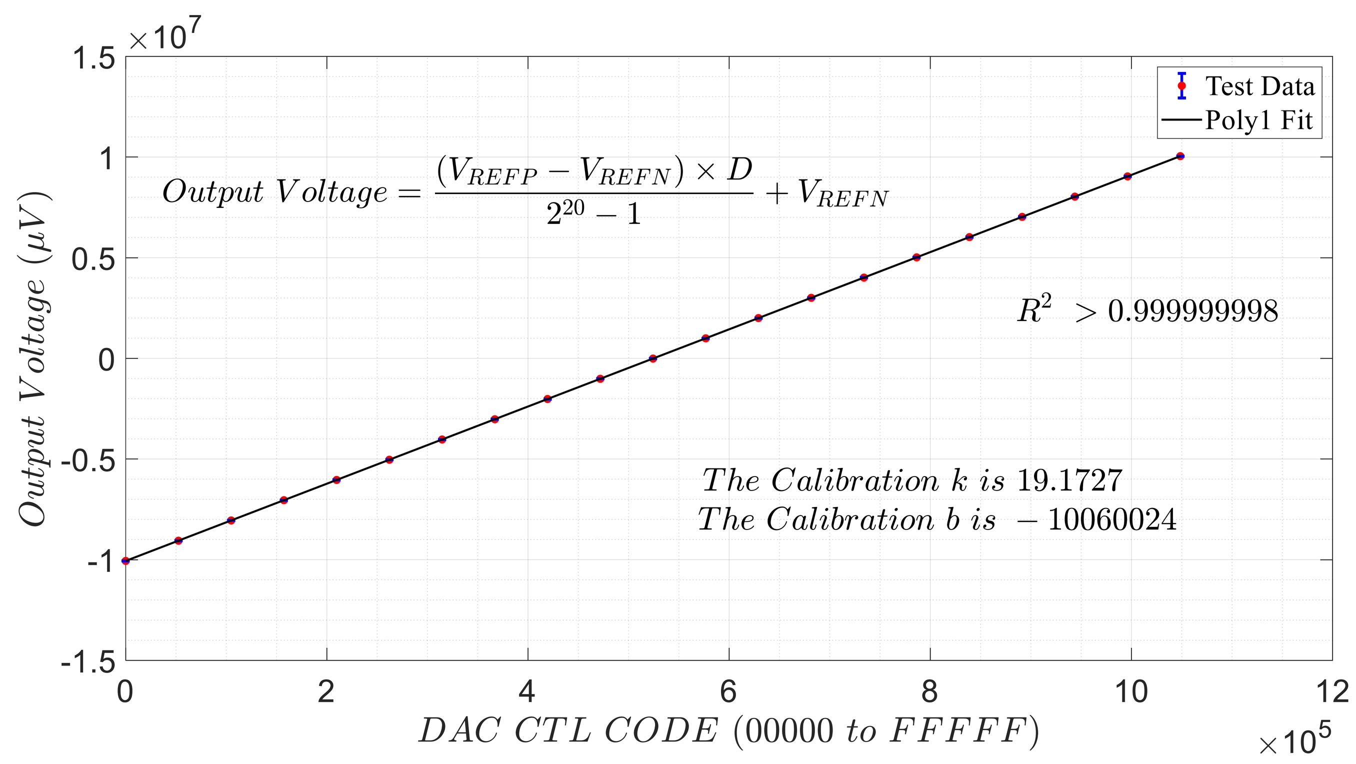


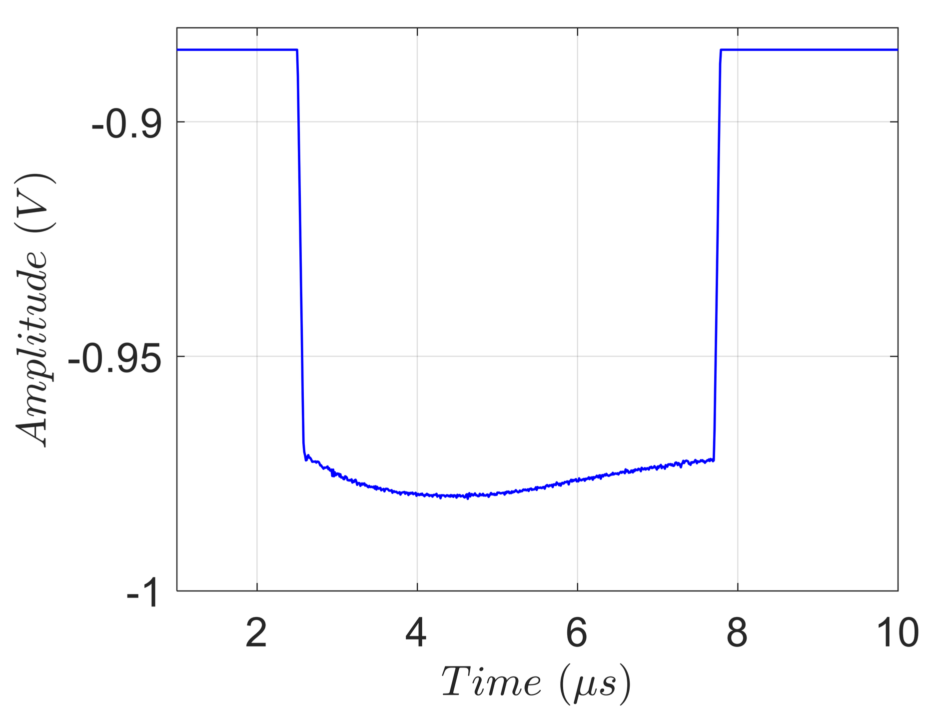
➢ Key Component Selection

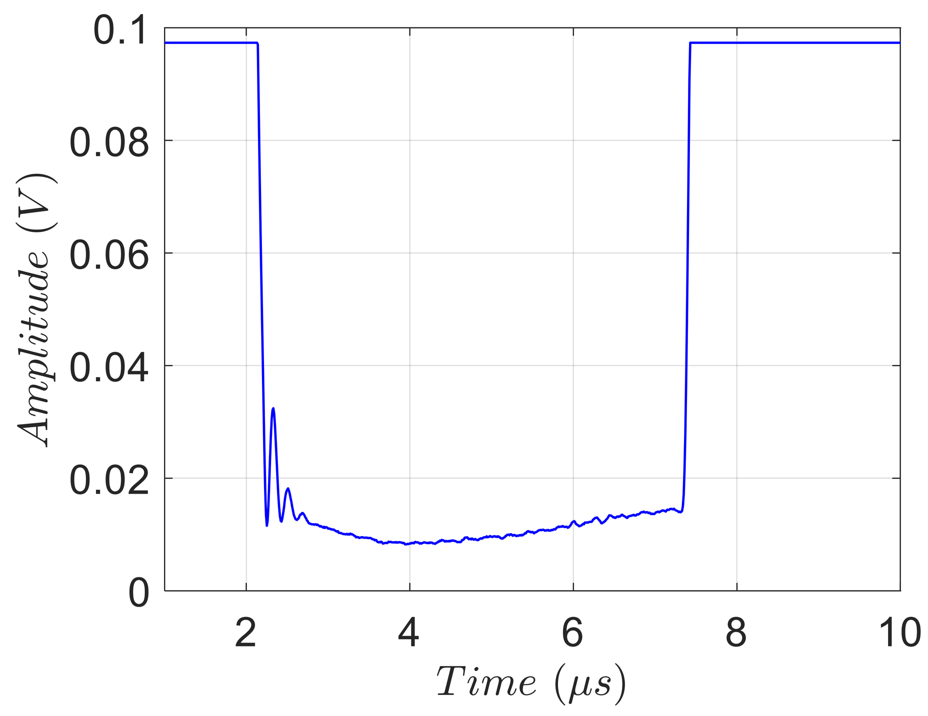
- ➢ A1, A2and A3: LT6018 from ADI
- ➢ Precision matched resistor network: LT5401
- ➢ DAC: 20-bit AD5791
- ➢ Reference voltage: LTC6655
- ➢ Buffer Amplifier: AD8676

➢ Test Result

- ➢ Output noise: $150.34 \pm 1.13\ \mu V$ RMS
- ➢ Supported measurement accuracy: 50 ppm
- ➢ Goodness of linear fit between DAC code and output voltage: 0.999999998
- ➢ DC bias adjustment capability: -10 V to +10 V







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