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A 20 Gbps PAM4 Receiver ASIC in 55 nm for Detector Front-end Readout

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With the continuous development in the high-speed optical data transmission systems for the detector front-end readout application, the PAM4 technique starts to emerge with its advantages of lower analog bandwidth requirement and less channel numbers.This paper presents the design and test results of a full-function 20Gbps PAM4 receiver ASIC fabricated in 55nm CMOS technology for detector front-end readout of high energy physics experiments.This 20Gbps PAM4 receiver ASIC mainly consists of an equalizer, a voltage shifter, 3 hysteresis-amplifiers, a decoder and a 10Gbps CDR.The voltage shifter shifts the common mode level of one PAM4 signal output from equalizer to obtain three PAM4 signals with different common mode levels for subsequent circuit decision and decoding.The 3 PAM4 signals output by the voltage shifter will be further amplified by 3 hysteresis-amplifiers respectively. Three MSDFFs (Master Slave DFFs) after the 3 hysteresis-amplifiers will resample the three signals and the sampling clock will be provided by the 10GHz clock recovered by CDR. The sampled signals will be sent to decoder for processing to obtain two NRZ signals. The PAM4 Receiver ASIC has been designed in 55nm CMOS technology with the chip area of 1.4mm×2mm.The full-chip post-layout simulation results show that two 10Gbps/ch NRZ data (MSB/LSB) can be correctly received and decoded from the 20Gbps PAM4 signal with a simulated ISI jitter of 1.3ps and 2.6ps, respectively. This PAM4 receiver ASIC has been taped out and the chip test will be conducted in one month, the results will be presented and analyzed in the full paper.

Minioral

Yes

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No

Are you a student?

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