Design of a 14-bit 40MSPS Pipeline Regional ADC for Monolithic Active Pixel Sensors

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Introduction

- As the leading research platform of heavy-ion science in China, the heavy-ion physics and heavy-ion applications at the Heavy Ion Research Facility in Lanzhou (HIRFL) and the High-Intensity heavy-ion Accelerator Facility (HIAF) which drive the development of new detector technology.
- Various applications at HIRLF and HIAF require Monolithic Active Pixel Sensors (MAPS) to measure the energy deposition, the hit position, and the arrival time of particle hit.
- As the critical component of this MAPS, a 14-bit 40MSPS Pipeline regional ADC converts the analog energy and time signal from the pixels into digital data.

The Architecture of the Pipeline ADC

Figure 1 shows the architecture of this regional pipeline ADC. The pipeline ADC is designed as a fully differential architecture and applies the redundancy correction algorithm and the structure of SHA(sample-and-hold)-less. The ADC consists of a 3.5-bit first-stage circuit and four 2.5-bit/stage circuits, and it ends with a 3-bit FLASH ADC. In addition to the main circuit, the two-phase non-overlapping clock generator, the bias current generator, and the delay correction module have also been designed.

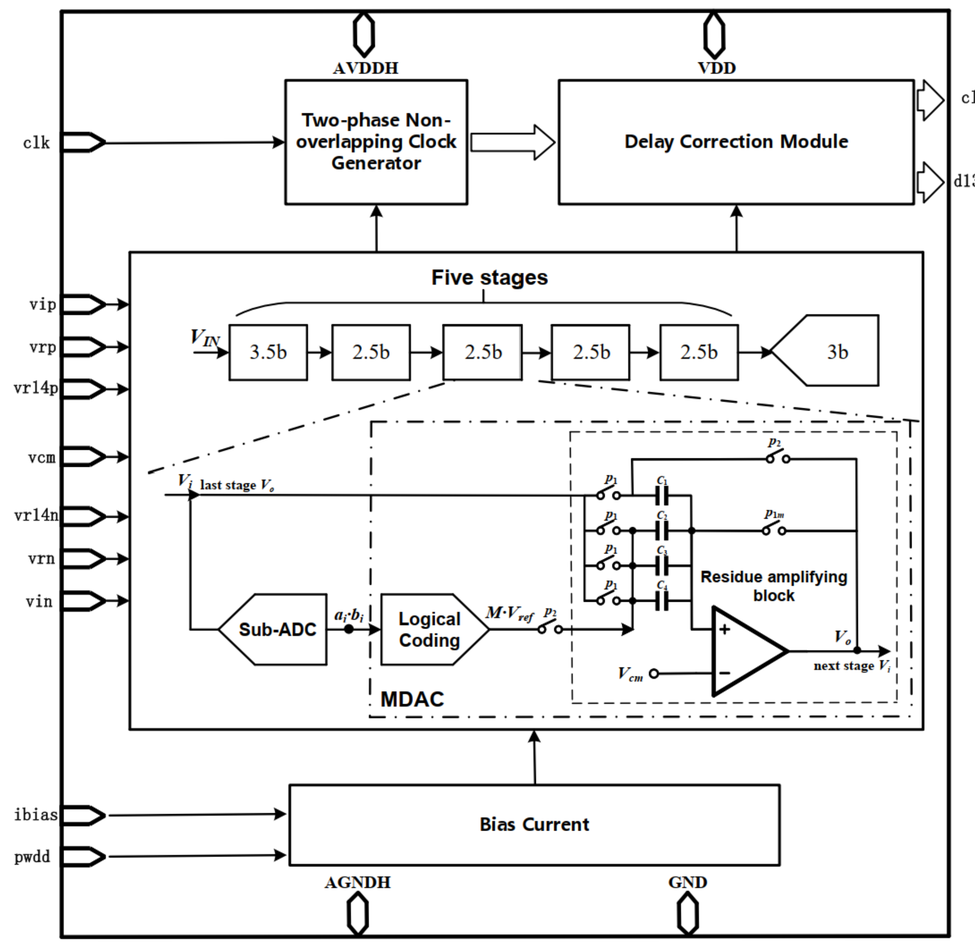


Figure 1. Structure of the pipeline ADC

Circuit Design Details of each Stage

Each stage circuit mainly includes two parts: a sub-ADC(SADC) and a multiplying digital-to-analog converter (MDAC).

- The resolution of the first stage circuit is 3.5bit, and the remaining four-stage circuits use a 2.5-bit structure.
- Bootstrapped switches are used to sample the varying input signals in the SADC and the MDAC in the first stage.
- **Figure 2 shows the Structure of the comparator.**
- **Figure 3 shows the Structure of the first-stage MDAC circuit on one side.**

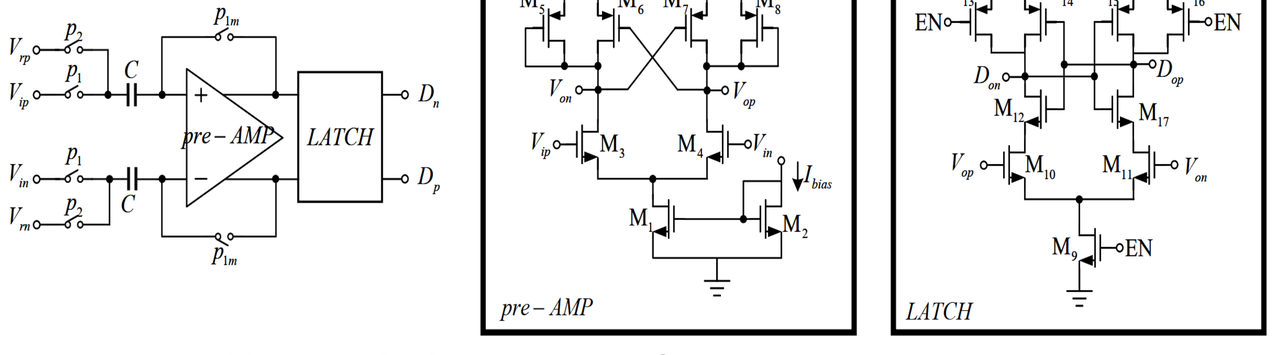
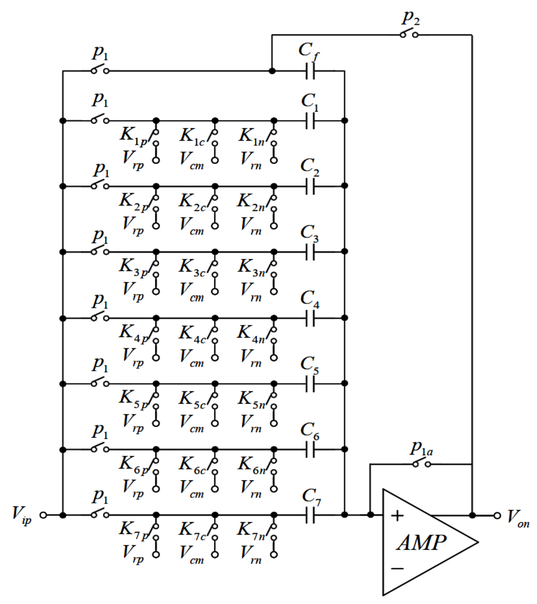


Figure 2. Structure of the comparator



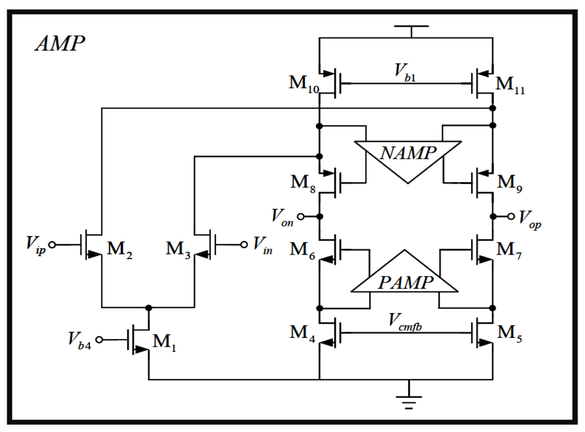


Figure 3. Structure of the first-stage MDAC circuit on one side

Results

Figure 4 shows the layout of the core of the pipeline ADC, which occupies an area of 1380μm×1300μm. **Figure 5 demonstrates the performance of the regional ADC.** The SFDR is 98.60dB, the SINAD is 83.36dB, and the ENOB is 13.56-bit.

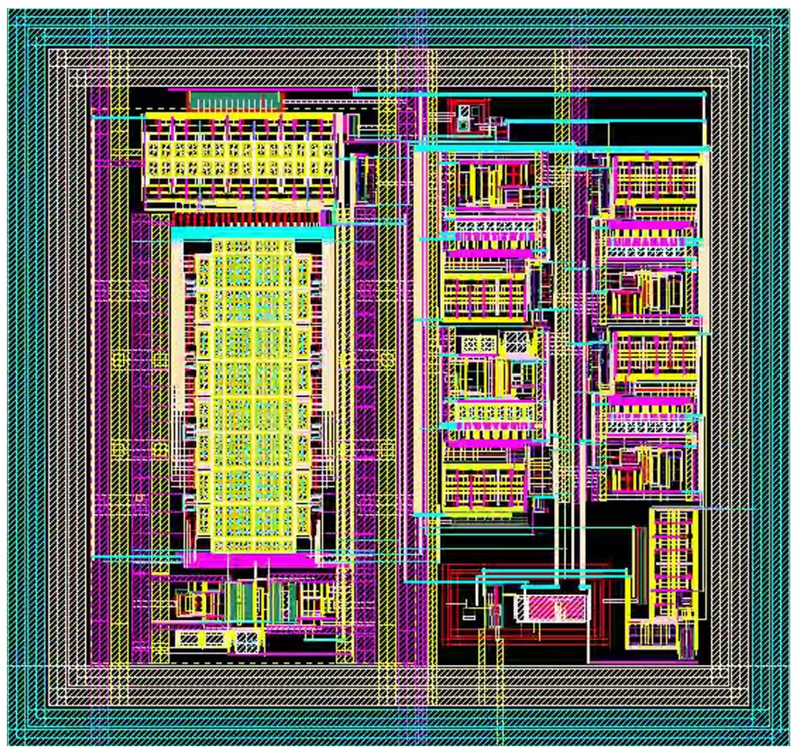


Figure 4. The layout of the core of the pipeline ADC

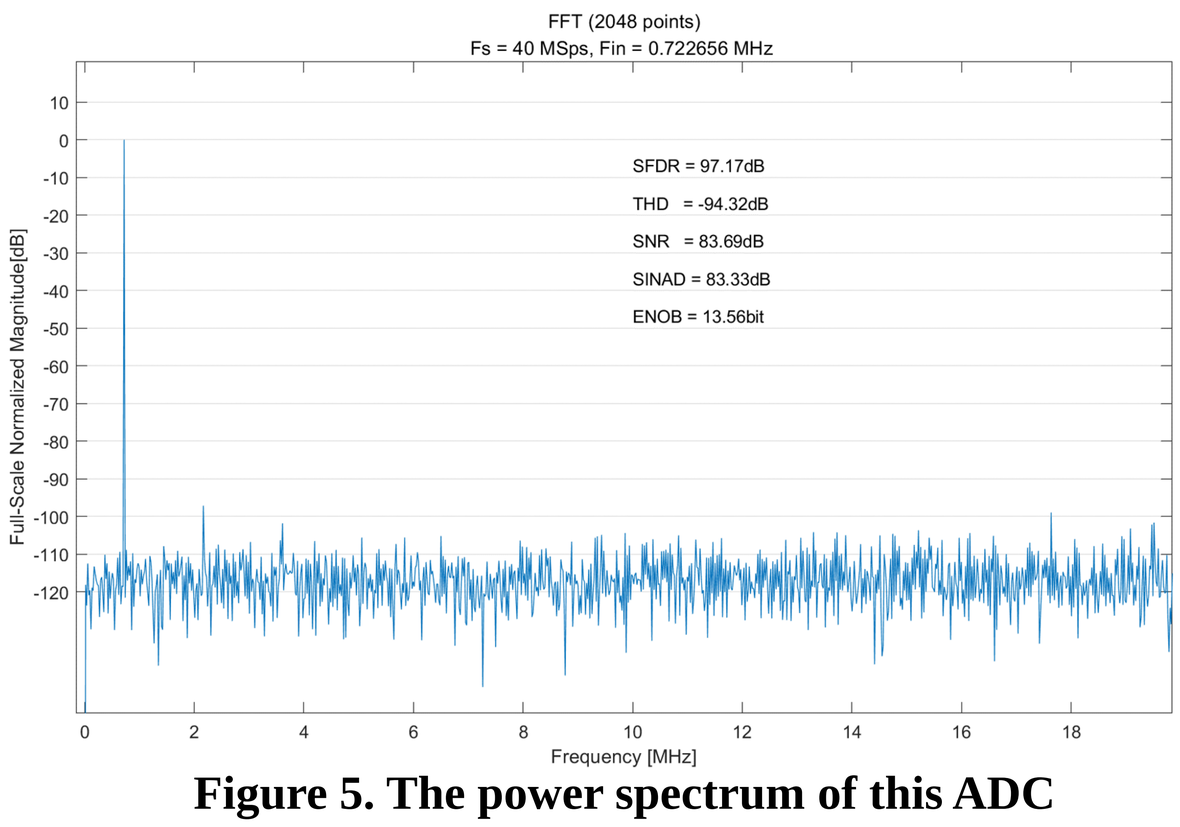


Figure 5. The power spectrum of this ADC