Time readout electronics for Semi-digital Hadronic Calorimeter (SDHCAL)

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Introduction

The CALICE Semi-Digital Hadronic Calorimeter (SDHCAL) is designed to be a high-granularity hadronic calorimeter for the future ILC experiments[1]. However, close-by showers can raise confusion in energy reconstruction for lack of time information. To address this issue, the Timing-SDHCAL has been introduced. This approach involves replacing some GRPC layers with MRPC layers to provide high-resolution time information of the hadronic showers. This enables the identification of neutral and charged particles and separation of close-by showers[2]. Here we present a prototype of timing electronics with two Petiroc2B ASICs and 64 channels, demonstrating a satisfactory timing resolution better than 100 picoseconds in injection tests.

Front-End Board

The electronic system consists of an FEB (Front-End Board) and a DAQ based on Zynq (SoC & FPGA)

- SMA for injection tests
- LTM4644 for power
- Si5345 for clocks
- 64 metal pads for picking up MRPC signals

The FEB is based on Petiroc2B, from OMEGA[3]

- Time resolution (TAC): 70 ps rms
- Readout time: ~ 12 us
- Power consumption: ~ 6 mW/chn

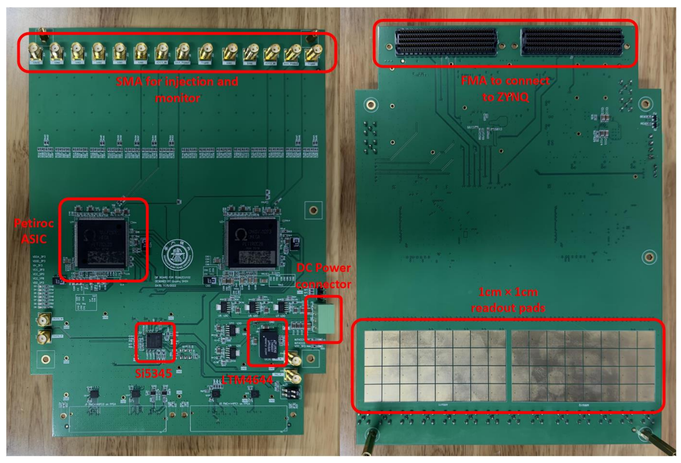

Fig 1 Front-end board

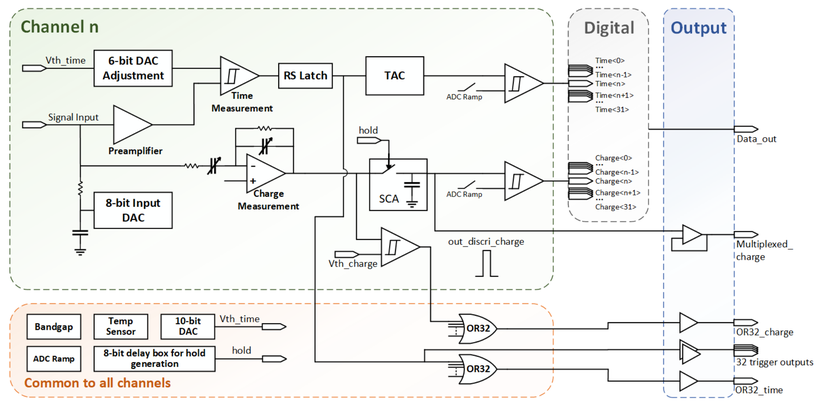

Fig 2 Block diagram of Petiroc

DAQ System

Programmable Logic (PL): traditional FPGA

- Slow control & configuration
- Data receiving & packaging
- FIFO, AXI logic cores, DMA, configuration logic core and readout logic core especially designed for Petiroc2B

Processing System (PS): embedded ARM processor

- low-level software
- I^2C applications
- LwIP (Lightweight IP) applications
- DMA controller

GUI software on PC

- Generating configuration data
- Communicating with PS via Ethernet
- Controlling the FEB
- Plotting S-Curves & implementing calibration

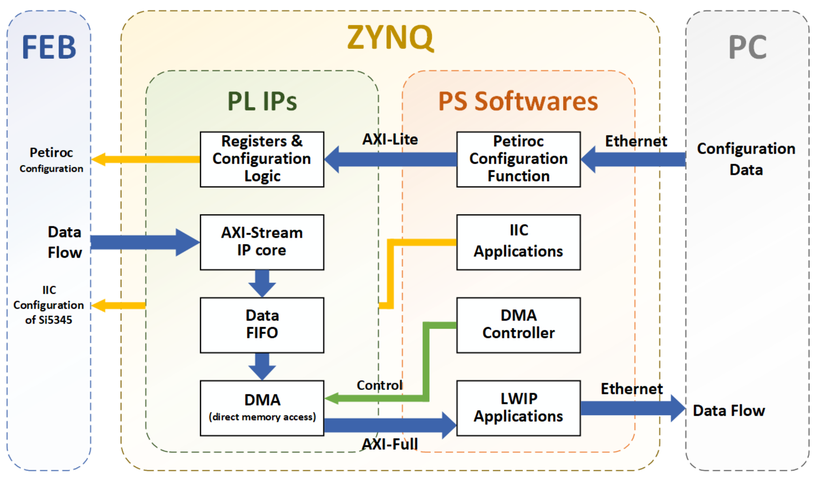

Fig 3 Diagram of the hardware

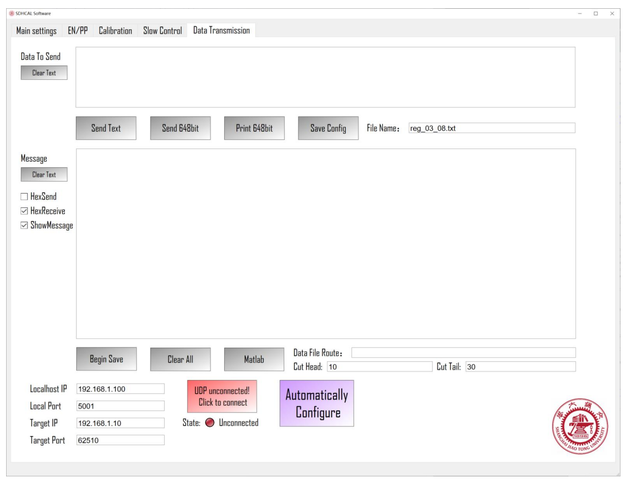

Fig 4 Picture of software UI

Calibration

The trigger threshold is composed of two parts: A 10-bit DAC global threshold and 6-bit DAC individual thresholds:

*Threshold Voltage = 0.89V + [(10-bit DAC value * 0.92mV] − (6-bit DAC value * 1.5mV)]*

Calibration for the uniformity of the thresholds:

- "S-curves" can be obtained on the pedestal
- RMS of 50% trigger rate threshold voltages: 9.4mV → 1.6mV

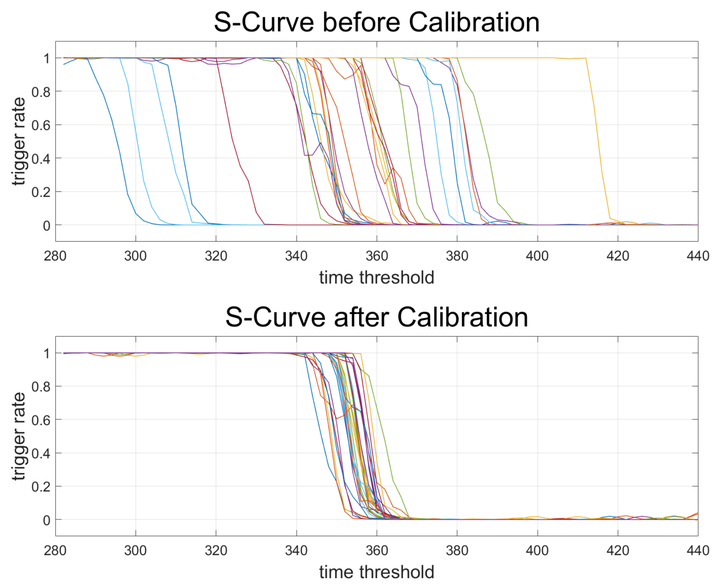

Fig 5 S-Curves before and after calibration

Timing Performance Evaluation Results

Periodic pulse waves of frequency 20kHz are injected to ASIC1 and ASIC2. Two tests were operated to obtain the timing performance:

- Measuring time differences between every two neighbor events with injection into one channel
- Measuring time differences between two ASICs with injection of identical signals
- RMS of timing between neighbor events is ~50ps
- RMS of timing between two ASICs is ~100ps

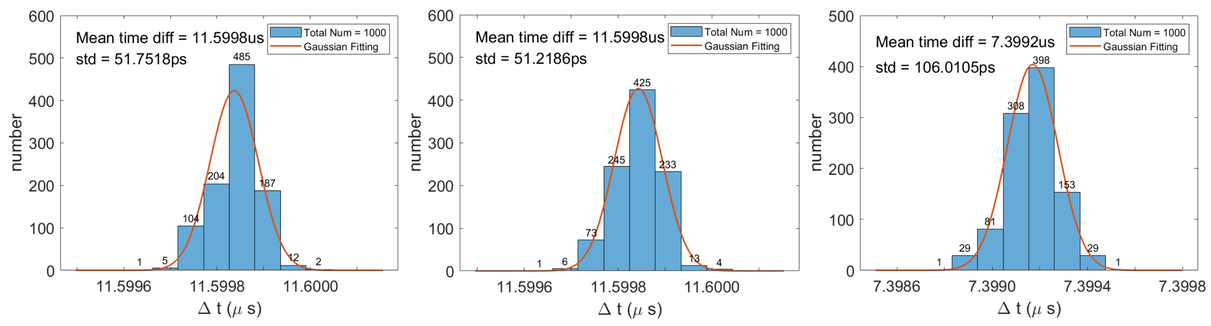

Fig 6 Results of injection tests.

Left: neighbor hits - ASIC1; Mid: neighbor hits - ASIC2; Right: same hits between ASICs

References

[1] Guillaume Baulieu, M Bedjidian, K Belkadhi, J Berenguer, V Boudry, P Calabria, S Callier,E Calvo Almillo, S Cap, L Caponetto, et al. Construction and commissioning of a technological prototype of a high-granularity semi-digital hadronic calorimeter. Journal of Instrumentation,10(10):P10039, 2015.
[2] Akchurin, N., C. Cowden, J. Damgov, A. Hussain, and S. Kunori. "On the use of neural networks for energy reconstruction in high-granularity calorimeters." Journal of Instrumentation 16, no. 12: P12036, 2021.
[3] Julien Fleury, S Callier, C de La Taille, N Seguin, D Thienpont, F Dulucq, S Ahmad, and G Martin. Petiroc, a new front-end asic for time of flight application. In 2013 IEEE Nuclear Science Symposium and Medical Imaging Conference (2013 NSS/MIC), pages 1–5. IEEE, 2013.