The Data Acquisition System of WEST's New Thomson Scattering Diagnostics

Christophe Bouchand, Yassir Moudden, Eric Delagnes, Thomas Chaminade, Alain Barbuti, Mathieu Carole, Gilles Colledani, Nicolas Fedorczak, Alexandre Magnino, Gilles Moureau, Roland Sabot, Loic Schiesko, Benoit Vincent and the WEST team

***Abstract*—WEST, the Tungsten Environment Steady state Tokamak at IRFM (France), is currently being equipped with two new plasma-monitoring systems based on Thomson Scattering. Nearly fifty optical viewing lines will be installed to collect scattered light near the core plasma region and in the plasma pedestal. The collected light pulses are forwarded along optical fiber bundles to polychromators where they are optically filtered into five channels and converted to swift electrical pulses. A custom fast digitizer board adapted to the polychromators was designed to capture these signals. This Nectarine board provides six triggered fast channels to catch the scattered pulse shape at 1 to 3.2 GS/s thanks to three Nectar chips. Six additional ADC channels provide a slower sampling rate for background monitoring. This contribution describes and discusses the performances of the real-time data acquisition and processing system, especially the Nectarine board, designed specifically for WEST's new Thomson Scattering diagnostics.**

***Index Terms*—Tokamak, Thomson scattering, plasma control, data acquisition, real-time systems, switched capacitor circuits, ring sampler, Field programmable gate arrays, system-on-chip**

I. Introduction

WEST, the Tungsten Environment Steady state Tokamak at IRFM (France), is currently being equipped with two new plasma-monitoring systems based on Thomson Scattering (Fig 1). This plasma diagnostic relies on the fact that the intensity and the spectrum of the scattered fraction of photons from an incident LASER pulse, holds information on the density and temperature of electrons in the plasma. The latter are two important parameters for plasma physics and real-time plasma control. Four optical viewing lines were installed on WEST late 2023 and first measurements were made during the C9 experimental campaign which lasted from January to April 2024. By the beginning of the C10 WEST experimental campaign in September 2024, it is expected that an additional 46 optical viewing lines will be installed to collect diffused light near the core plasma region and in the plasma pedestal. With the use of both simple and multiplexed fiber bundles, the result is 40 optical channels to be converted thanks to 40 polychromators.

E. Delagnes and T. Chaminade are with the Université Paris-Saclay, CEA, IRFU, 91191, Gif-sur-Yvette, France (e-mail: eric.delagnes@cea.fr).

All other authors are with CEA-IRFM, 13108 Saint-Paul-Lez-Durance, France (e-mail: christophe.bouchand@cea.fr , yassir.moudden@cea.fr).

These will spread the input light into 5 spectral bands resulting in as many as 180 high-speed data acquisition channels. In order to provide a cost effective integrated high performance fast digitizer solution, a decision was made to design a custom board befitting the needs of the chosen polychromators. The board was named Nectarine after the Nectar chip it is based on.

A short description of WEST's Thomson Scattering diagnostics (TSD), including Lasers and polychromators, is given in section 2. Section 3 provides an overview of the Nectar Chip and of its essential features as well as motivations for its use in the fast pulse acquisition channels of WEST's TSD. Section 4 describes the Nectarine in house electronic board design, its architecture and its functionalities. Lab performance measurements and experimental results obtained on WEST during the C9 campaign are gathered in sections 5. Conclusions and perspectives are outlined in the final section.

II. WEST's NEW TSD

The design of the new high resolution TSD on WEST is reported in [11]. The goal is to deliver high precision and high resolution measurements for plasma physics, for example to study heat flow to the divertor and the dynamics of the high confinement regime in the core region. Enhanced plasma control is also targeted and so the system should also be able to output estimates of physical quantities such as electron density and temperature profiles in real time. Fifty lines of sight are being installed along the laser beam (Fig. 1): 38 on the plasma edge with ~6mm resolution (16 multiplexed and 6 simple fiber bundles), 20 for core plasma measurements with ~25mm resolution combined into 10 multiplexed fiber bundles, and 4 more needed for laser alignment which adds another 2 multiplexed fiber bundles.

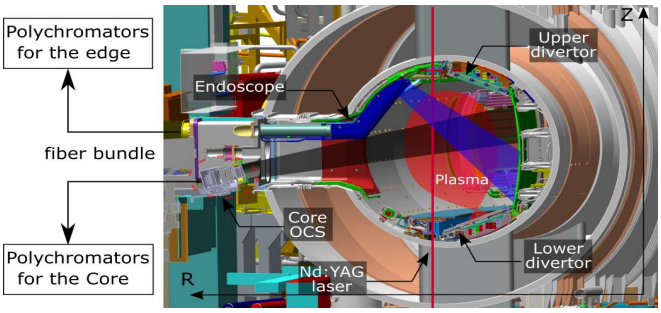

Fig. 1. Cross section of the WEST Tokamak, showing the lines of sight of the new Thomson Scattering Diagnostics

Both core and edge optics and mechanics have been designed with great care to enhance light collection and signal to noise ratio, as well as to screen the greater part of in vessel reflections. The long pulse objectives of WEST implied stringent mechanical and thermal specifications. Actively cooled components and shields were used to protect the optics from the plasma. In fact, to meet the requirements for edge measurements, a dedicated actively cooled endoscope was designed [11].

Two SpitLight 2000-2500 Nd:YAG Lasers procured from Innolas [17] are currently installed on WEST's TSD. Both lasers can deliver 2J of monochromatic light pulses at 1064 nm in very short pulses of a few nanoseconds, at a maximum repetition rate of 30Hz. The Lasers offer different triggering options, either internal or external. They will eventually be used synchronously for higher energy pulses or alternately for higher firing rate hence time resolution. The laser path and light dump are equipped with cameras, pyroelectric sensors and photodiodes to provide the necessary monitoring to control mirror angles and to answer safety requirements.

The scattering of the laser photons on the free electrons (the incident wavelength being well below the Debye length of collective electron phenomena) is the fundamental process by which electron properties in the plasma such as temperature and density are probed. Thus the shape of the measured scattered light spectrum, which is Doppler shifted due to electron velocity, reflects the temperature of the electron distribution. The intensity of the scattered light, after proper calibration, is then linked to electron density. However, the intensity of this scattered light remains relatively low and several other phenomena, treated as noise, contribute to the acquired data: Rayleigh diffusion, background emission, bremsstrahlung, etc.

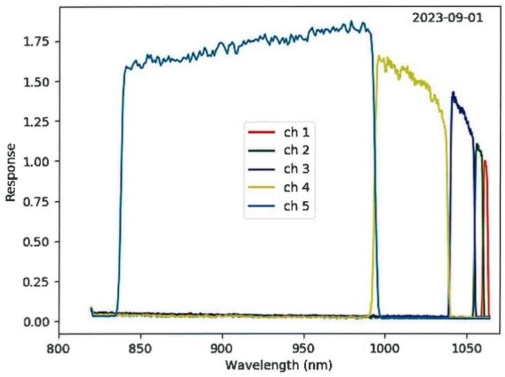

Fig. 2. Spectral response of the five optical filters of one of the 36 polychromators between 840nm and 1070nm.

For both diagnostics, core and edge, single or duplexed fiber bundles channel the collected scattered light to polychromators in charge of optically separating the photons in 5 wavelength intervals. This is achieved thanks to specific narrow band Fabry-Perot interference filters covering the 840ns nm top 1070nm wavelength range (Fig. 2). Filters and incident wavelength were defined based on WEST plasma properties to enhance background noise reduction. For the WEST TSD, polychromators were procured from UKAEA [2]. Inside the polychromators, APD based photo detectors, that are temperature stabilized for gain control, convert the intensities of the spectrally resolved scattered light into swift nanosecond electrical pulse waveforms. Practically, the preamplifier output is divided into two channels, low pass LF and high pass HF respectively for background and pulse measurements with different requirements regarding digitization.

Many options were investigated searching for a proper digitizer and data acquisition solution for WEST's new TSD. Modularity, mechanical integration and interfaces to both the polychromators and the backend, were important requirements. Also, considering that around 36 polychromators will be installed resulting in around 180 HF channels and as many LF channels, cost was a major concern. Obviously, the most important features driving the design are the very low 30Hz laser trigger rate on one hand and the very high GS/s sampling rate required to catch nanosecond pulse waveforms. Designing a custom electronic board to provide each polychromator with six Nectar fast digitizer input channels, six slower channels for background measurements and the necessary programmable resources for data readout and possible local real time processing, seemed the most cost effective solution. Finally, downstream of a local gigabit network, the data acquisition system includes back-end PCs to gather and further process the acquired waveforms.

III. Nectar Chip

Although the cost of fast digitizers has been sliding during the past years under the pressure of the highly demanding RF communications industry, the availability of waveform sampling solutions with subnanosecond time resolution for most other applications, especially in experimental physics, remains a challenge in many respects. Cost is obviously a difficulty, as is very high-speed electronic board design which requires very specialized training, skills and tools.

For the needs of WEST's TSD and its foreseen 180 measurement channels, several options were considered: full commercial hardware solutions based on possibly interleaved flash ADCs with commercial software leaving little room for customization seemed out of reach compared to lesser expensive commercial boards based on switched capacitor arrays (SCA) (e.g. [19]). To further reduce expenses as well as try to mitigate the risk of obsolescence on the most significant components a decision was made to design a custom board based on the Nectar chip, a SCA developed at CEA/IRFU [4]. This option appeared to be the best in order to keep full expertise within the lab on the long run, as well as the best at providing the ability to add and upgrade functionalities in software and firmware such as embedded distributed preprocessing of the recorded pulses for real time applications.

The basic principle behind the SCA solution (Fig. 3), is to do without expensive fast ADCs in two steps. First, the input waveform is memorized as analog amplitudes into an array of capacitor cells, switching from one cell to the next at the high sampling rate. For instance, the propagation of a slow clock along a calibrated delay line can provide the necessary fast virtual clock [16]. Then, on reception of a trigger pulse one can proceed to the postponed conversion of the analog samples

through a cheaper low conversion rate ADC [16].

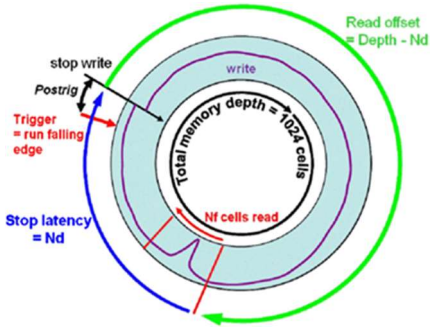

Fig. 3. Schematic view of the Nectar 1024 cell SCA circular memory operation.

For TSD, data acquisition is triggered at the same rate the Laser is shot through the plasma. This feature is further in favor of an SCA fast sampling solution since there is no requirement for sampling the inputs continually. The adequacy of SCA fast samplers for TSD had been identified in a previous proposal for TSD upgrade on Tore Supra [9] where it was proposed to use the Matacq chip and MatacqVME board [21]. More recently the DRS4 chip [20] was used on a custom board for the data acquisition of TSD on GDT [10].

Nectar is the latest of several SCA designed at IRFU: ARS and SAM are previous generations used in challenging astroparticle physics experiments such as ANTARES [24] and HESS [22]. Nectar was designed to fit the fast digitization needs of the ~2000 channels of each camera on the larger telescopes of the Cerenkov Telescope Array [1,4,5] and was also used on a HESS upgrade [23]. There is a major difference in the nature of the trigger signal between TSD and astroparticle experiments. For the latter, the trigger is random and the depth of the analog memory is used to buffer the data while the trigger is computed. Also, to reduce deadtime due to SCA readout, to maximize trigger rate, only a limited number of cells are read out. However, TSD uses the LASER trigger: it suffices to properly delay that trigger to catch the scattered light pulse of interest. And, the trigger rate is limited by the Lasers' capabilities to a few 100 Hz.

Compared to all of the previously mentioned SCA chips, Nectar has the distinctive feature of including an ADC which greatly simplifies board and firmware design as well as more compact placement when required (Fig. 4).

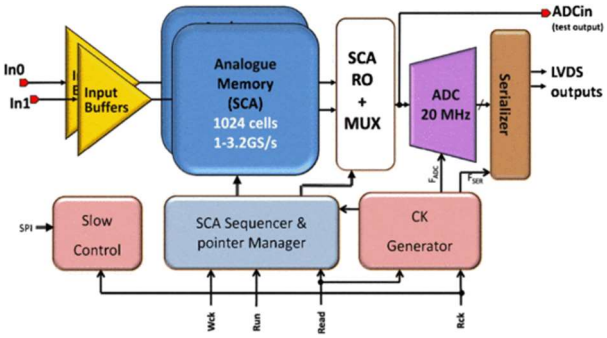

Fig. 4. Synoptic of the internal architecture ASIC-NECTAR2

The major properties of the Nectar chip (Fig. 5) are [16]:

- 800 MHz to 3,2 GHz sampling rate
- 1024 cells
- between 320ns and 1.3µs recording time
- Readout deadtime ~300µs for 1024 cells at 1 GHz
- 20 MHZ ADC, 12 bits resolution
- 2 channels per chip
- Slow control, debug mode
- Dynamic range ~1.2V
- Analog bandwidth ~400 MHz
- low cost plastic QFN 100 casing, 0.35µm technology
- power consumption: 210 mW per chip

For high precision applications, all the components on the measured signal path display dispersions that need to be accounted for. In the case of Nectar, as with other SCA, the concern is with dispersions between chips but also between the internal constituents of the array: gains and offsets along lines or columns of the capacitor matrix, time intervals between sample locking, etc. All of these can be calibrated. The Nectar also includes several features to correct offsets affecting amplitude or the linearity of the time scale [16]. In fact 32 DACs are included to adjust offsets on the 16 lines of the capacitor array. Different reset strategies are implemented on the DLLs of each column of the SCA and expert control of the DLLs is available to finely tune each column delay [16]. Also, there is also an option to read out the number of the first cell read, or to constantly read out the SCA from a specific cell index. This is useful for calibration procedures. For the first measurements delivered by TSD on WEST during the C9 campaign, an off-line procedure was retained for offset corrections.

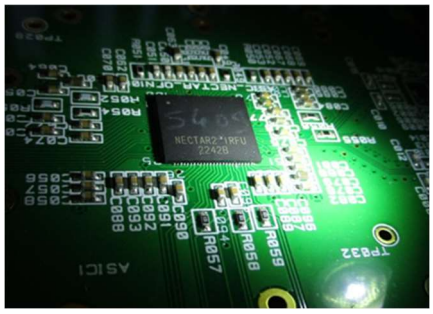

Fig. 5. View of the NECTAR chip on the NEcTARINe board.

IV. NECTARINE BOARD

The Nectarine board (Fig.7) was designed with a tight fit to the polychromators: the 19 inch board is housed inside a 1U casing. It presents 12 SMA connectors on its front panel for 6 HF and 6 LF channels. Three additional inputs are for clock, trigger and timer reset. Three Nectar chips implement the fast digitization needed for the 6 HF channels. Input signal conditioning is achieved using a single to differential amplifier circuit based on the LTC6409 chip [14] with a gain of 2, to compensate for the 50Ohms input impedance. To adjust the gain to actual polychromator output dynamics, the modification of resistors and capacitors is required. Three differential pairs

are routed for Nectar readout allowing optional implementations in firmware. Slow control is implemented separately on each Nectar.

Digitizing the LF channels relies on the LTC2500 [13]. The latter provides 24 bit sensitivity, several on chip digital filtering options, adjustable sampling rate up to 1MHz. With digital filtering, the output sensitivity reaches up to 32 bits. For physics analysis, the LF channels provide measurements of the background emissions which add to the diffused laser pulses.

A Zynq 7020 System-on-Chip (SoC) from Xilinx [Fig 7] is used for the Nectar and ADC slow control and readout. In fact, the Nectarine board was designed as a baseboard for Avnet's Microzed module [6] according to the guidelines [25]. This low cost design option greatly and reliably simplifies and accelerates the design of the digital functions of the system since it avoids the placement and routing of high-speed components including SoC, DDR, etc.

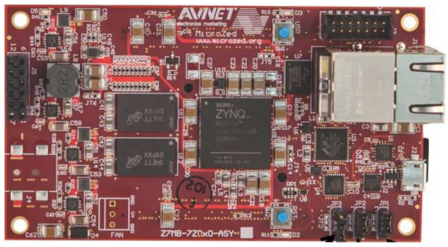

Fig. 6. Microzed System on Module including a Zynq7020 System on Chip from Xilinx.

The main features of the Microzed module (Fig. 6) used in this design are as follows:

- 1 GB DDR3 (x32)
- AMD Xilinx Zynq 7020 MPSoC
- 10/100/1000 Ethernet
- 32 GB Micro SD card interface
- JTAG
- 100 single ended I/O - 48 LVDS pairs
- USB UART bridge

During WEST operation, the server racks, housing the polychromators, Nectarine boards and backend PC, are no longer accessible hence remote hardware reset options have been implemented. Each port of a remotely controlled ethernet power switch is used to bring power to each Nectarine board. Another self-reset option is to use a software driven Zynq output, delayed using proper components on board to drive the power sequencing circuit. A final option is to use a proper combination of signals on the Clock , Trigger and TimerReset inputs, driven by the backend PC to address a specific Nectarine board and order a firmware reset.

Great care was taken in the design of the power circuits and each board is powered from its own very low noise linear source. Different voltage levels on the board need to be sequenced for proper operation. Power on sequencing, guidelines for mother board design are given in [25].

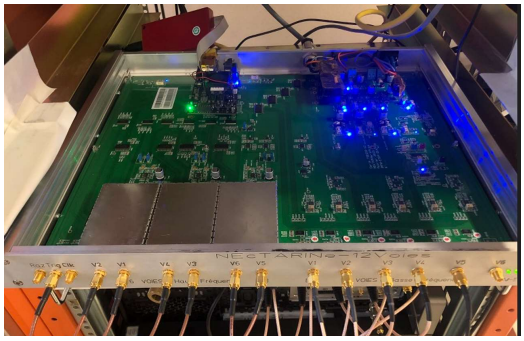

Fig. 7. View of the NEcTARINe board

V. NECTARINE FIRMWARE & SOFTWARE

Developments targeting the Zynq SoC include firmware to configure the chip's programmable logic (PL) and software to run on the chip's processing system (PS).

The firmware implements the necessary logic blocs to read and write to the slow control registers on the Nectars, to control data sampling into the SCA and to control the serial protocol to read it out through the ADC of each Nectar. The three Nectars are read-out in parallel resulting in 300µs deadtime for 1024 samples read on each chip. The trigger signal is handled without re-clocking hence with very low additional jitter to keep as deterministic a trigger latency as possible for a more efficient data read-out and analysis. The firmware also implements logic to configure and control the ADCs on the LF channels. The 6 LF channels are sampled simultaneously which allowed sharing and saving several I/Os on the Microzed. Several modes are available for LF sampling including free running periodic sampling at a rate configurable in the Zynq.

Precise and coherent timestamping of the trigger events on the RF channels as well as of the data samples from the LF channels is achieved using a 48 bit counter and a free running 100MHz clock. This clock can either be from a local oscillator or common to all Nectarine boards depending on the global timing precision needed in the end. Subnanosecond precision trigger timestamping [15] is also achievable if needed for even higher precision resynchronization of waveform measurements, from different channels and different boards along the laser's path through the plasma. Otherwise, should the dynamics of a trigger driven event be irrelevant, reducing timestamp precision to a small multiple of the laser trigger frequency would be enough for unequivocal event building.

Firmware blocks (Fig. 8) were developed using Xilinx's Vivado IP packager as AXI peripherals with memory-mapped registers for control and monitoring. A true dual port memory is also included in each block to transfer data between PL and PS. When needed, its constitutive block rams were specifically reconfigured and rearranged to reorder data bits after PL writing and before PS reading operations. The true dual port memories are organized into circular paged buffers. PL and PS share page pointers and permissions in a very basic protocol through regular peripheral registers.

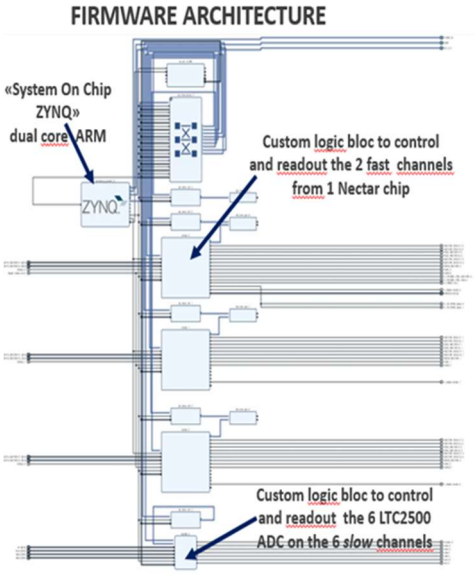

Fig. 8. Block architecture of the firmware targeting the ZYNQ system, including control and readout logic for the 6 HF and LF channels, as well as synchronization signals : Trigger, Clock and Timer Reset.

For now, the PS configuration and software is kept very simple. Only one of the two ARM cores is used and it is used in standalone mode without operating system. The lightweight IP library (lwip) [8] is included in the Xilinx/Vitis project to efficiently manage standard Ethernet communication protocols with the backend PC. The second ARM core will be added when needed, for instance when more involved data processing is required in the real-time plasma control loop.

The standalone software implements a TCP/IP client for slow control and configuration. The Nectarine's mac and IP addresses are built from its identifier index stored in the on board flash along with other Nectarine specific parameters (e.g. the common mode on each Nectar inputs is set with a DAC and using stored value). All configuration operations of the Zynq PL, the Nectar and other configurable parts on the Nectarine can be accessed remotely via TCP/IP as well as locally through a standard serial console on the usb connector. This channel is also used to periodically check connectivity and if necessary to automatically execute client /server connection retrials. Trigger enabling before the Laser is started and disabling after the Laser has been stopped is also done through this channel. In the end, firmware and software are combined using Xilinx's design tools into a BOOT.bin file stored on a microSD card from which the Zynq can start up.

Data transfer to the backend PC uses UDP frames. On a small private network of point-to-point links, this is very safe and provides higher throughput. The data from the Nectar chips and the ADC are streamed to the backend PC for further processing, storage or display. The current end-to-end latency has not yet been assessed. If faster transfer is needed on the front end side, custom memory cache management and/or DMA could provide some relief.

VI. Backend System Architecture

The backend data aggregating PC runs TCP/IP and UDP servers. At this time, its main purpose is to configure the connected front-end Nectarine boards, and write the received data to a file in the HDF5 format. It will be fully integrated within the WEST framework [3] for the upcoming C10 WEST experimental campaign, possibly including on-line event building routines and subsequent temperature and density estimator algorithms for plasma real time control.

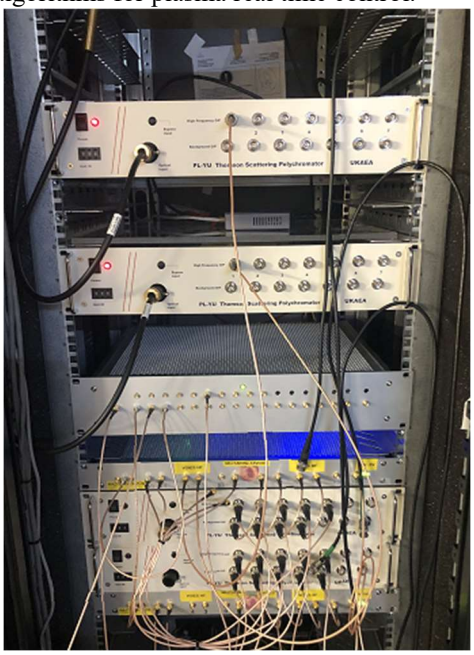

Fig. 9. Equipement of two polychromators and two NEcTARINes for the first tests acquisition and alignement on TSD.

Eventually, the full system will consist of 36 polychromators and associated Nectarine boards. The total data flow from the currently 5 active HF channels on each Nectarine is expected around 200 Mbit/s which should be sustainable on a single Gb/s Ethernet link and is well below the capacity of the PC's internal PCIe bus. However, there is some uncertainty due to the non-standard nature of the triggered data flow [12]. Since it was decided to use COTS hardware on the backend, the different Ethernet switches needed to funnel the data down to the backend PC will be chosen based on buffer depth on the inputs which is not a specification made systematically clear on datasheets. In all cases, the backend is relatively modular, flexible and expandable: if needed, the number of networking boards inside the backend PC can be increased and a second or third backend PC could also be added.

There is no definite decision made at this time given that only two modules were operated during C9 (Fig. 9). Full scale tests will be conducted prior to the beginning of the next experimental campaign in September 2024 for a full assessment of the backend hardware performance.

To complete the TSD data acquisition architecture, a dedicated board was designed for trigger, clock and timer reset distribution. The design relies on the NB3l553 clock multiplexer [18] that operates just as well on short trigger or reset pulses. The board multiplexes each of its three inputs to

16 outputs. Care was taken during placement and routing to reduce output latency dispersion. In order to achieve fast signal distribution to as many as 40 Nectarine boards, a two stage tree is needed requiring 4 boards.

The trigger signal to the Nectarine boards should be bound to the LASER. The Nectar chip requires a trigger after the laser pulse is recorded in the SCA hence deriving the trigger signal from light falling on the laser dump is the preferred solution and it should be operational for C10. For now, a slightly downgraded solution was implemented based on the Laser's Pockel Cell Sync output. The jitter compared to the actual Laser output measured using a photodiode, is approximately 4 ns. Jitter was inevitably added by the digital delay line inserted on the trigger path to produce the post trigger needed by the Nectar chips.

The polychromators, Nectarine boards, fast signal distribution modules and Ethernet switches are all installed in three thermoregulated server rack. Thanks to the embedded temperature measurements on the Zynqs, a broad temperature map will be derived as soon as all the Nectarines are installed in the cubicles. The measured temperature dispersion maps will determine if additional efforts are needed in designing a more homogeneous cooling system.

VII. Results

The two Nectarine boards for the C9 experimental campaign were first qualified in the lab before they were installed in the Tokamak Hall in the TSD cubicles to perform real measurements on plasma. Obviously, the electromagnetic conditions in the Lab and in the cubicles are very different. Noise levels measured in the lab are at least 2 to 3 times lower.

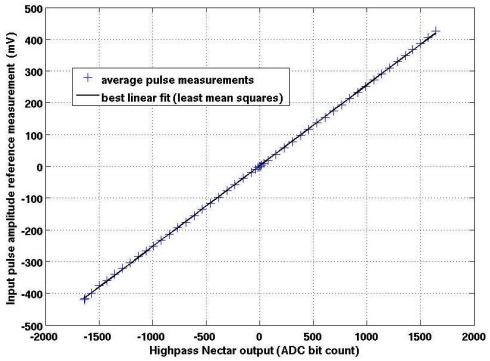

Fig. 10. HF channel linearity

A. Laboratory measurements

A precision voltage generator Keithley 2450 was used to assess the linearity of the HF and LF channels of the Nectarine board. Figure 10 shows the results for a single Nectar channel on one of the two tested Nectarine boards. A large number of constant voltage steps were taken over the channel's dynamic range. Output mean and standard deviation were computed at each step. A linear least squares fit provided the reference characteristic. The standard deviation from the linear fit for the HF channel is 2.31mV which corresponds to 0.27% of the full scale, which is in close agreement to the expected performances given in the technical report [16]. All 6 HF channels on both boards display comparable performances.

Similar results for the 6 LF channels of the same Nectarine are shown on figure 11. The standard deviation from the linear fit for the LF channels is 2.64mV which corresponds to 0.053% of the full scale again in close agreement with the expected performance given in the datasheet [14].

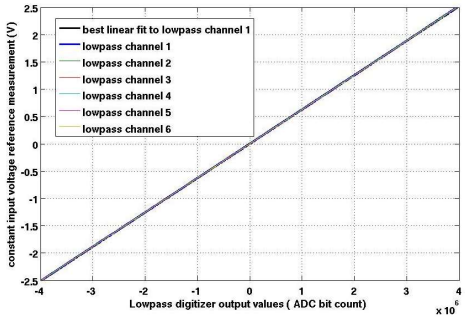

Fig. 11. BF channel linearity

The noise standard deviation on the HF channels, measured either with an open circuit, a 50 ohms endcap or a short circuit, is roughly the same. Figure 12 shows a histogram of output amplitudes for open input. The estimated noise standard deviation is 1.7 ADC counts meaning that the ENOB on the HF channels is 11. Based on the previous linear transfer function, the sensitivity on the HF channels is approximately 420µV much better than the requested 10 mV sensitivity for scattered light pulse detection.

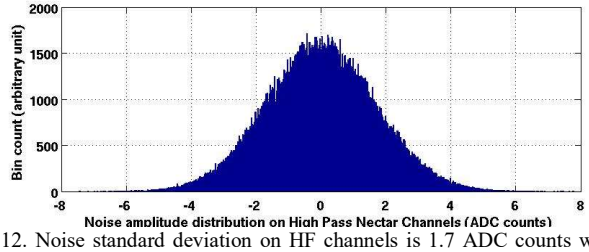

Fig. 12. Noise standard deviation on HF channels is 1.7 ADC counts which converts to ~ 420µV

Similar results for the LF channels are shown on figure 13. The estimated noise standard deviation is 53.6 ADC counts, resulting in an ENOB equal to 18. Using the previously computed linear characteristic, the sensitivity on LF channels is approximately 34.7 µV.

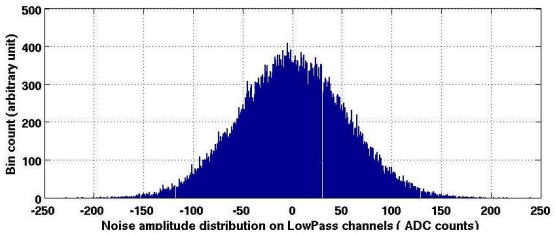

Fig. 13. Noise standard deviation on LF channels is 53.6 ADC counts which converts to ~ 34.7µV

B. Experimental data on West plasma

Typical data from the five HF channels of one of the two polychromators and Nectarine operated during C9, are shown on figure 14. The full 1024 cells of the Nectar chips are read out; the first 640 cells are used to estimate the 16 cell long pattern of offsets to be subtracted. The successive pulses correspond to two lines of sight: the two fiber bundles are brought together with a difference in length into a single sheath and into a single polychromator. The time difference between the two pulses is obviously related to the different lengths of the two multiplexed fiber bundles. Longer optical paths through the polychromators for successive channels are also visible in the sampled waveforms.

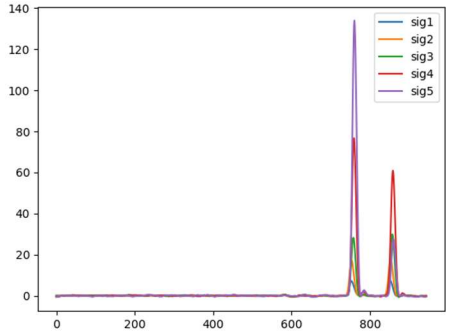

Fig. *14*. Typical acquired HF raw data pulses acquired on the 5 HF channels during a plasma experiment on WEST.

Figures 15 top and bottom show recordings over a 60 second plasma discharge of the 5 LF and HF channels on the same time scale provided by the 48 timestamps of all LF samples and HF triggers. For the HF data, only the maximum amplitude of the first pulse is given. For multiplexed data, the LF channels cannot discriminate background from either line sight.

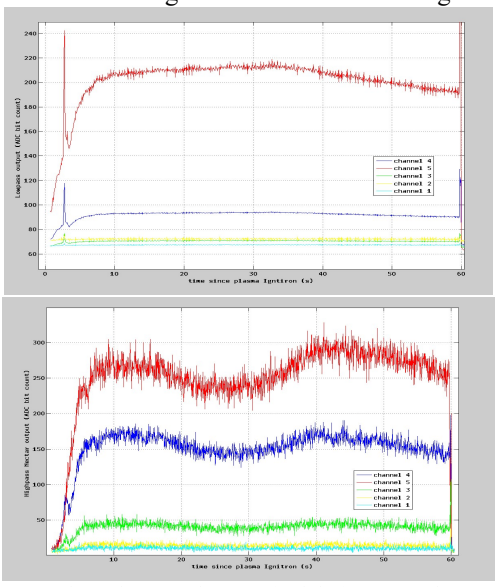

Fig. 15 LF (top) and HF (bottom) data acquired during a 60s plasma discharge on WEST during the C9 experimental campaign.

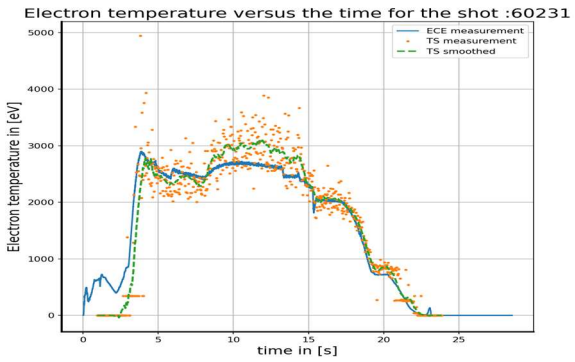

Fig. 16. Estimated lectron temperature estimated from the TSD data during WEST plasma shot number 60231, compared to similar estimates from the Electron Cyclotron Emission (ECE) data.

An offline preliminary analysis in Python of the acquired data files leads to an estimation of the temperature profile over the time of the plasma discharge in good relation with measurements from other diagnostics on WEST (Fig. 16). Similar studies for density measurements are ongoing. These encouraging results will be confirmed as the understanding of noise sources and physics algorithms are refined. An online implementation for plasma control is expected in the near future.

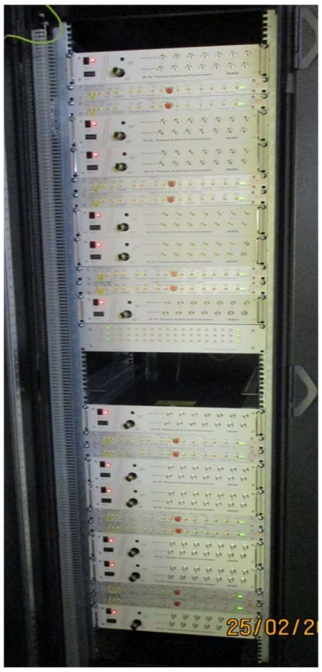

Fig. 17. The integration of 36 Nectarine boards and Polychromators in three thermoregulated cubicles for WEST's C10 experimental campaign is work in progress. .

VIII. Conclusions - Perspectives

First measurements were performed successfully all through WEST's C9 experimental campaign (first quarter of 2024) allowing some final tuning and system debugging in the very stringent Tokamak environment. Thanks to the designed data acquisition system's very low noise, high sensitivity and very high time resolution, the collected scattered light pulses on 4 duplex optical channels using 2 Nectarine boards could be

successfully used to estimate plasma electron density and temperature.

For WEST's C10 experimental campaign (Q4 2024) the full system will be installed: up to 36 Nectarine boards + polychromators inside three server racks (Fig.17). The backend hardware and software including ethernet switches will need some adjustment to accommodate the non-standard « triggered » data flow from the front-end boards. The embedded resources available on each Nectarine board and backend PC are being investigated for realtime electron temperature and density estimation for plasma control applications.

The good performances of the Nectarine board have attracted interest from other diagnostics on WEST. For instance, current developments also include customization of Nectarine boards for realtime reflectometry for plasma control on WEST. Another possible application of the Nectarine board is the acquisition of the very faint signals from bolometers used to measure radiative power losses. For the latter, the very low noise of the LF channels could provide a profitable upgrade of the current data acquisition electronics.

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