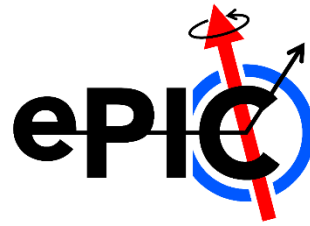
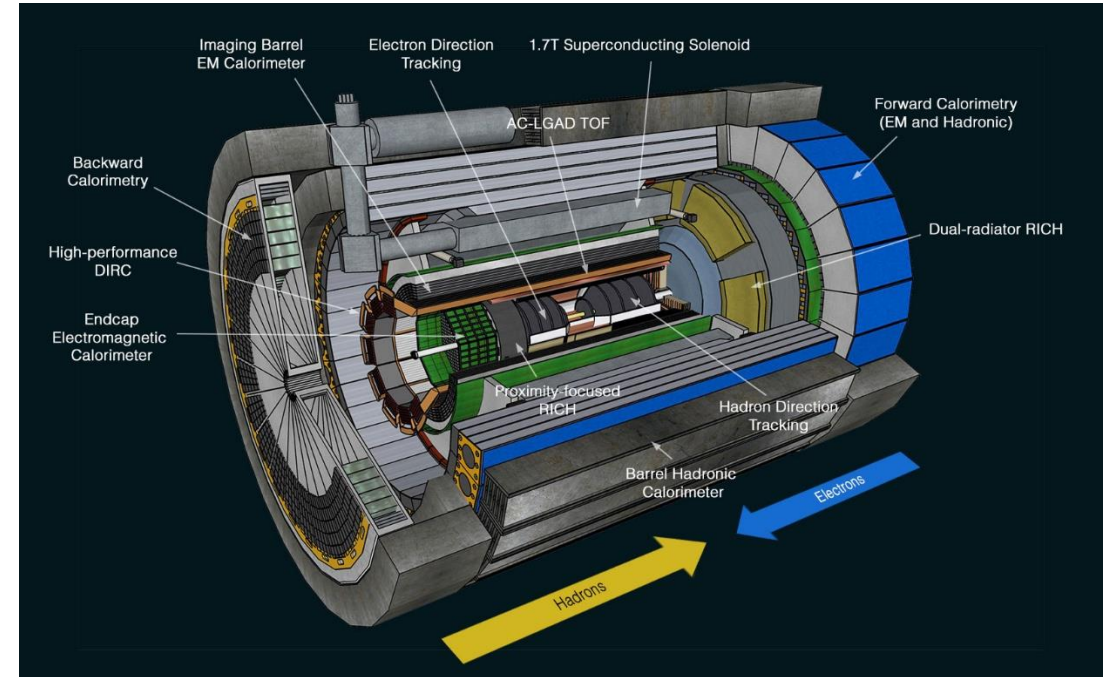
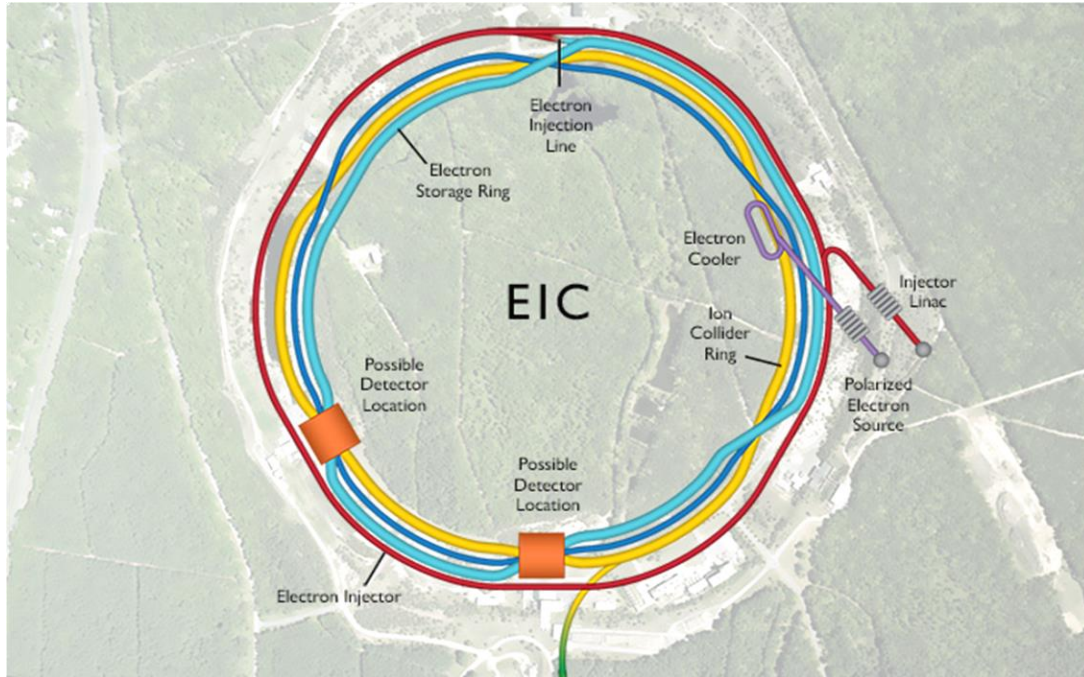


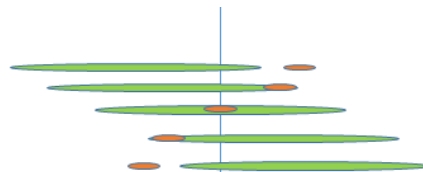
A Proposal for the Clock and Control Distribution for EIC Experiment (ePIC)



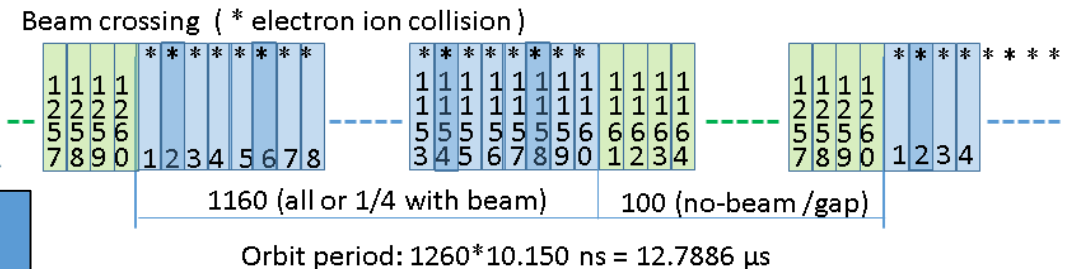
J. W. GU (for ePIC collaboration)



	ESR	HSR
RMS bunch length σ_z [mm/ps]	7-9/23-30	75-60/250-200
Electron Beam Energy: 5 – 18 GeV		
Proton Beam Energy: 41, 100, 275 GeV		
Luminosity: $10^{34} \text{ cm}^{-2}\text{s}^{-1}$		



Beam Crossing every 10.15ns, or 98.5 MHz



ePIC DAQ /Clock Control distribution electronics

GTU: Global Timing Unit

control encoding, status decoding.
The interface for machine clock source,
Data acquisition control and monitor etc.

DAM: Data Aggregation Module:

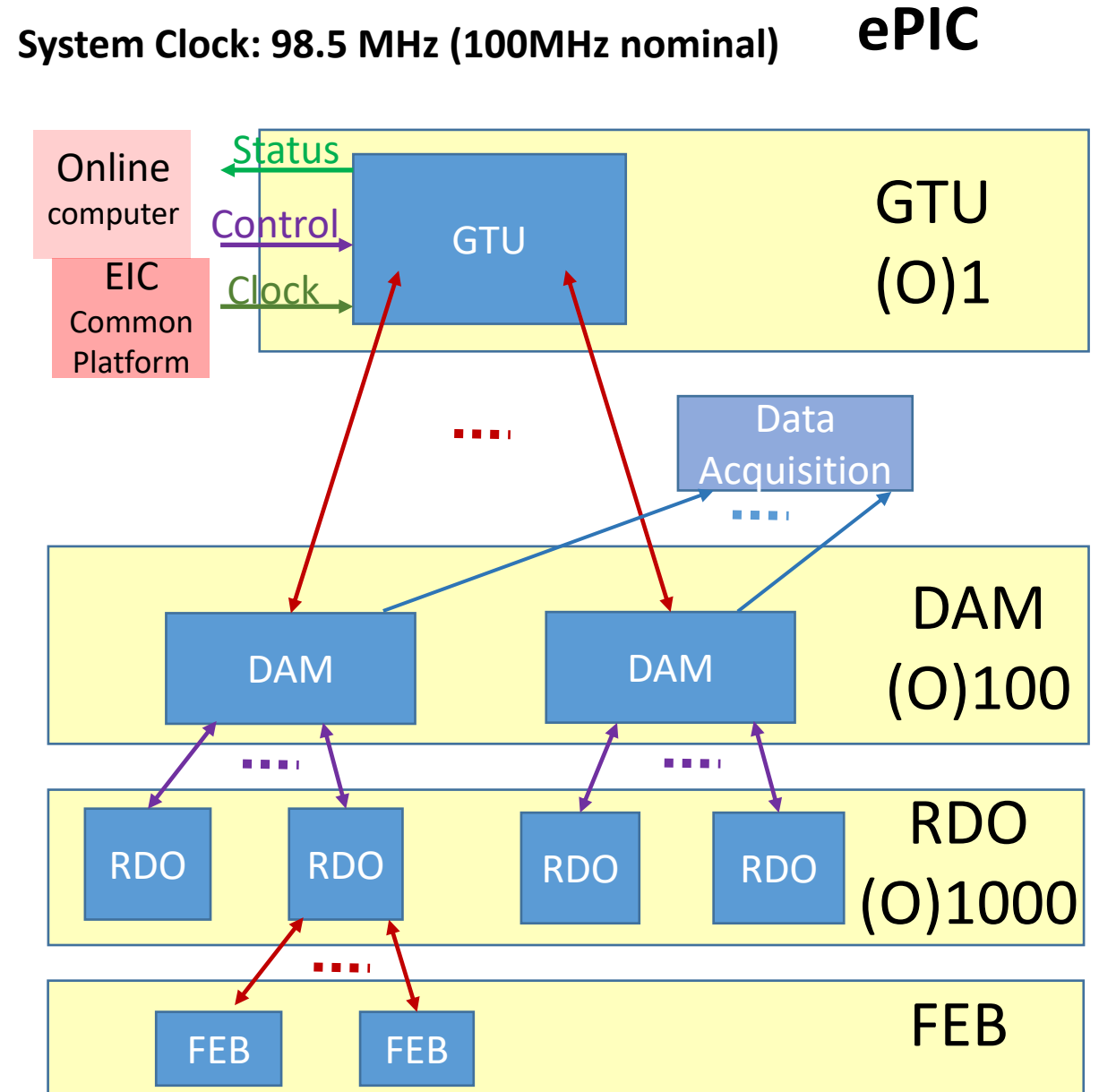
The clock/control fanout, and status/busy
accumulation.
local control over the RDO boards connected,
though the main function of the DAM is for Data
Acquisition.

RDO: optical interface of detector ReaDOut

control decoding, status encoding.
The clock/control interface to the front end
electronics.
Data collection from Frontend boards, and data
transmission to the DAM

FEB:

Detector dependent Front End / ASIC
carrier boards.



Clock Distribution

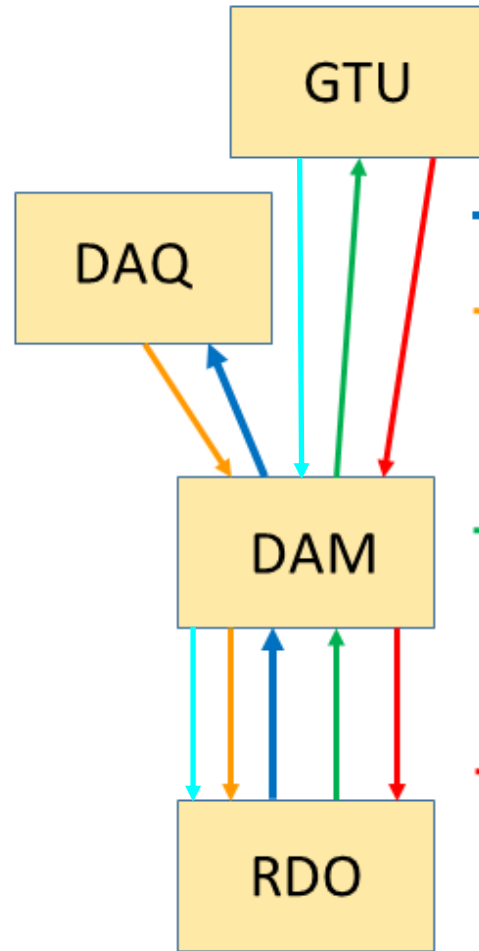
GTU fanouts:
Additive Jitter <1ps
Phase: fixed

Dedicated fiber
Additive Jitter <1ps
Phase: fixed

DAM fanouts:
Additive Jitter <1ps
Phase: fixed

Optic fiber cable:
Additive Jitter <1ps
Phase: fixed

RDO Rec Clock:
Additive Jitter <3ps
Phase: stable,
fixed with PseudoClock



→ Data flow

→ Data Buffer 'FULL' backpressure

→ Status accumulation: Data Buffer conditions, Out of Sync, Reset_request, etc.

→ Run_control: SRO_time_start/stop, RESETs, etc.

Beam Crossing phase aligned

Streaming ReadOut time windows:



Control Distribution

1. Introduction
The EIC (Electron Ion Collider) experiment, ePIC will be constructed and commissioned at P6 in BNL. This presents a low jitter and phase deterministic CLOCK, and synchronous CONTROL distribution system to the front end electronics. The design, some test results, and near-future plans are presented.

2. Hardware description
2.1 The diagram of ePIC DAQ, Clock /Control distribution electronics
2.2 Hardware description
GTU: Global Timing Unit control encoding, status decoding. The interface for machine clock source, Data acquisition control and monitor etc.
DAM: Data Aggregation Module: The clock/control fanout, and status/busy accumulation, local control over the RDO boards connected, though the main function of the DAM is for Data Acquisition.
RDO: optical interface of detector ReadOut control decoding, status encoding. The clock/control interface to the front end electronics. Data collection from Frontend boards, and data transmission to the DAM
FEB: Detector dependent Front End / ASIC carrier boards.

3. Clock Distribution
3.1 Dedicated fibers between GTU and DAM (and maybe RDO)
The GTU recovers the 98.5 MHz EIC beam crossing clock as the ePIC system clock. The clock is fanned out using ultralow jitter clock chips and optic transceivers on the GTU. The clock is received by the optic transceivers, and jitter cleaned and fanned out to the MGTs (Multi Gigabit Transceivers) on the DAM.
3.2 MGT serialized data between DAM and RDOs
The GTU_CONTROL (8-bit) and DAM_CONTROL (32-bit) are serialized and phase aligned with the System clock (98.5 MHz) on the DAM (fiber DOWNLINK). The RDO reconstructs the system clock, and sends front-end electronics data and status back to the DAM (fiber UPLINK).

4. Synced CONTROL Distribution
4.1 Fixed latency from GTU to DAM, and RDO
The fibers from GTU to DAM will be the same length/delay routed in the DAQ computer racks. The fiber delays from DAM to RDO will be measured individually, and saved on the RDO. The RDO will delay the received GTU control commands (compensating for the fiber latency), so that all the RDOs will send the GTU commands at the SAME time (synchronous with the 98.5 MHz system clock).
4.2 Beam orbit information is embedded in GTU control command
The GTU, DAM and RDO will all keep (at least) two counters, Beam Crossing counter (11-bit from 1 to 1260), and Beam Orbit counter (at least 5-bit, for a total time period of about 400 μs). The GTU will send SRO (Streaming ReadOut) time windows start command and some other SYNC commands on the first beam crossing of the orbit. The size of RDO time window can be set on the GTU.
4.3 DAQ data flow control
There are data buffers on DAMs and RDOs. The buffer status is monitored by GTU, DAM and RDO.

5. Some Test results
5.1 Test setup: Skyworks's Si5344H → System Clock, Reference BNL's FLX182 as DAM, OpaKelley's XFEM8320, Xilinx KCU105/Skyworks's Si5394A as RDO
5.2 (RDO's) RxRxClock Test setup: The clock jitter is measured by the positive width of the difference between the RxRxClock and the reference clock using the Tektronix's MSO64 oscilloscope.
6. Status and Future plans
6.1 Proved designs by others
TJNAF's 12 GeV upgrade program proved that the dedicated clock distribution and the DAQ (BUSY) feedback are viable.
6.2 Pre-prototype RDO is being manufactured
6.3 Prototype FLX155 (ePIC DAM) is expected this year
6.4 To setup a sub-system DAQ (DAM + RDOs) to fine tune the protocols, to think about GTU prototyping

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