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A Fully Reconfigurable Pipelined Architecture for FPGA-based Parallel PRBS Test Pattern Generators

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Serial links are widely used for data transfer in Data Acquisition (DAQ) Systems of High Energy Physics (HEP) experiments. Pseudo-Random Binary Sequences (PRBS) has seen wide application in high-speed serial wireline communication systems as test patterns for link characterization and testing. A flexible architecture for FPGA-based PRBS generators is proposed, with a focus on high throughput and full reconfigurability. In order to meet the demands of increasing data rates, the proposed architecture employs a parallel datapath with high scalability. The architecture is designed to be fully parametric and reconfigurable, which allows dynamic reconfiguration of all parameters of the PRBS generator on the fly, including polynomial, seed and output width. Reconfiguration of the parameters is achieved by simply writing to corresponding registers, without the need to re-synthesize or re-configure the FPGA device. A built-in bootstrap logic is used to convert parameter register values to internal states that are fed to the datapath to generate the output bit sequence. The datapath is pipelined to facilitate optimized timing performance on FPGA devices. The proposed design can be utilized to characterize serial link performance under a great variety of different test patterns rather than several selected ones, providing broader insights. The architecture is implemented in CHISEL and verified on an Intel Agilex-7 FPGA and a 106.25-Gbps serial link, where results show promising performance and scalability.

Minioral

Yes

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No

Are you a student?

Yes

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