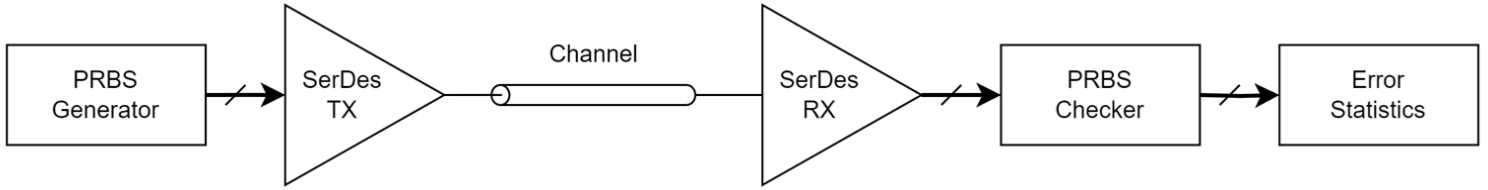
#165 A Fully Reconfigurable Pipelined Architecture for FPGA-based Parallel PRBS Test Pattern Generators

Chengyang Zhu, Kezhu Song, Dongwei Zou, Zhuo Chen

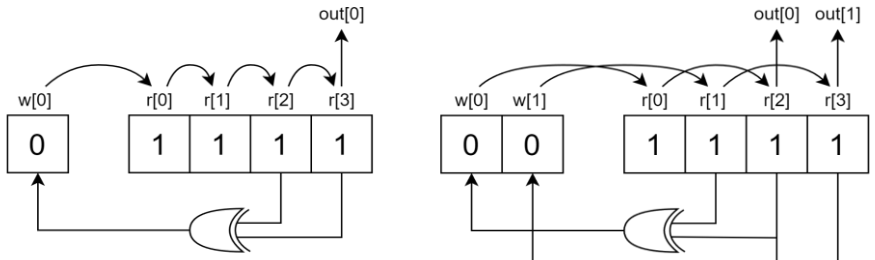
Serial link error testing with PRBS



What is PRBS?

- Deterministic bit sequences with random-like statistical behavior
- Can be easily generated and checked

Basic structure of a PRBS generator



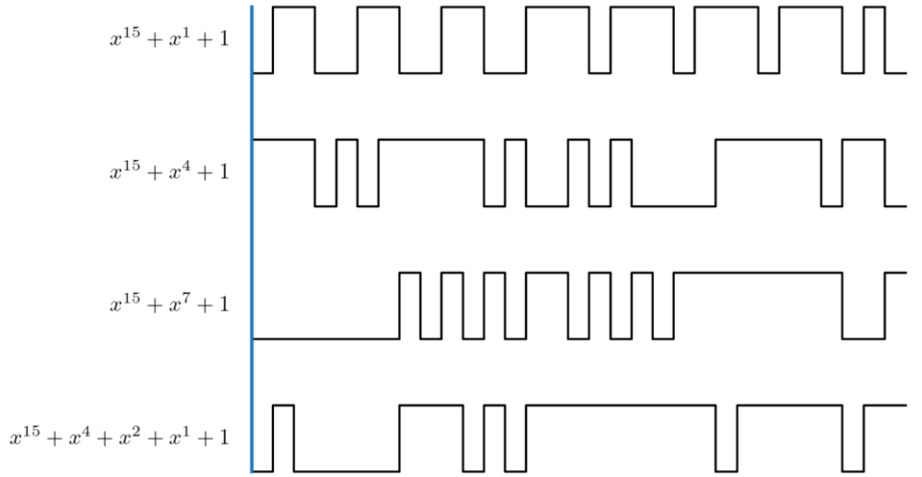
(a) serial

(b) 2-wide parallel

Example shown:

- **Order:** 4 (hence PRBS-4)
- **Polynomial:** $1 + x^3 + x^4$
- **Seed:** 1111
- **Width:** 1(a); 2(b)

PRBS waveforms



Waveforms generated with:

- Same order
- Same seed
- Different polynomials

Shows differences in baseline wander, clock content, etc., resulting in different error behavior from the link under test

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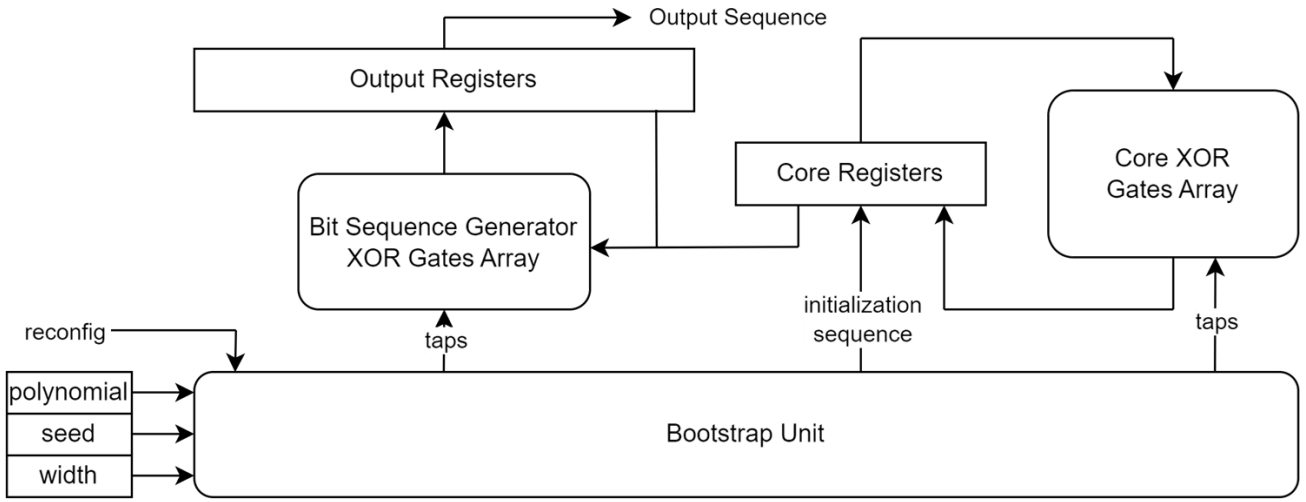
Objective

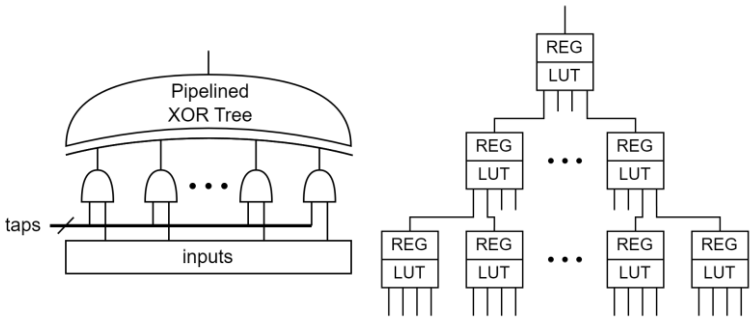
A new architecture for PRBS generators to facilitate fine-grained control over test patterns

- **Flexible:** runtime reconfigurable parameters
  - Order
  - Polynomial
  - Seed
  - Width
- **Scalable:** reasonable complexity, timing optimized
  - Larger width for higher throughput, with comparable Fmax

Proposed architecture



Building blocks



maxWidth	Fmax (Mhz)	Throughput (Gbps)
16	552	8.83
32	571	18.28
64	560	35.83
128	574	73.48
256	552	141.36

Results