Study of Decoupler: Empowering FPGA Debugging with ESP32 and IoT

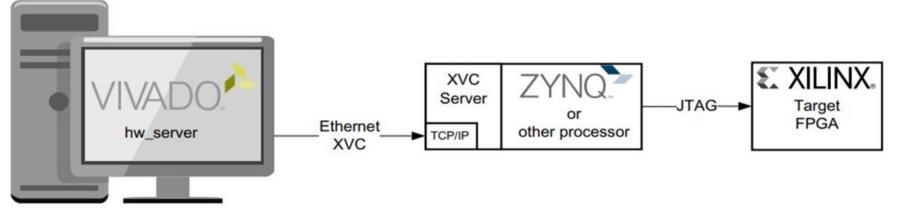
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Common features of high energy physics experiment electronics system

- Front-end electronics(~1000s of channels).
- Back-end electronics(~100s of boards).
- Large number of custom designed FPGA based PCBs.
- Either easy or difficult to access after installation.
- Require constantely parameter monitoring before and after installation at low frequency(~minutes).

Limitations of traditional solution





By implementing remote configuration and environment monitoring independently :

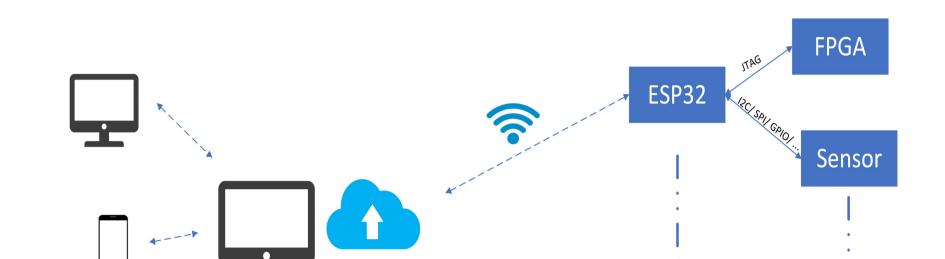
1. Decouple the core function design with peripheral functions such as environment monitoring.

Decoupler

2. Decouple the installation with maturation of the firmware design.

Key advantags:

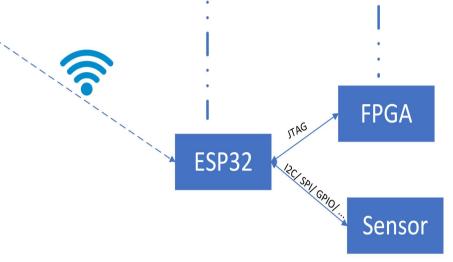
- Better security and reliability.
- Lower logic and PCB



- Using JTAG programmer at early stages.
- Remote configuration and slow control system at late stages.
- Solution requires extra logic and space resource and not available at the beginning.

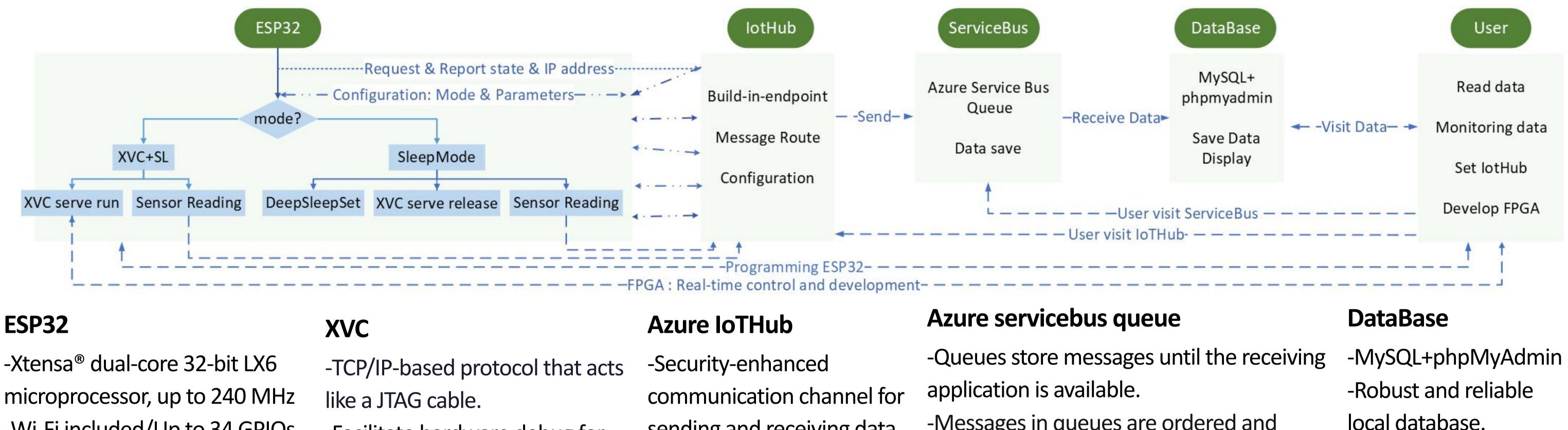
resource.

- Less material and power consumption.
- Easier maintainability and
 scalability.



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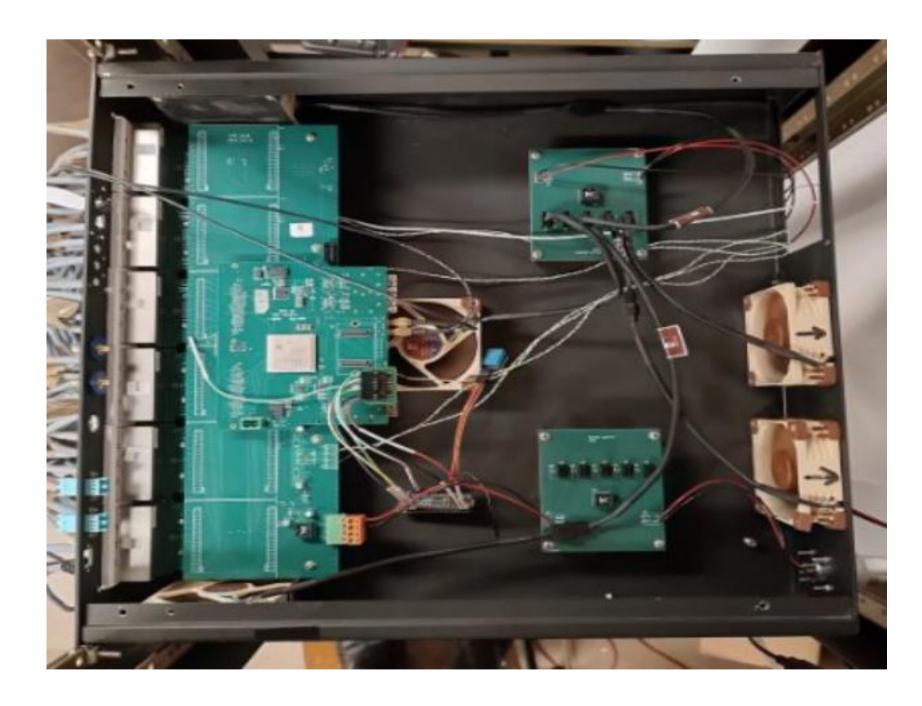
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-Wi-Fi included/Up to 34 GPIOs	-Facilitate hardware debug for	sending and receiving data	-Messages in queues are ordered and	local database.
-As IoT device send data to	designs that: have the FPGA in a	from IoT devices.	timestamped on arrival.	-Insert data
IoTHub	•	-Route message to different	-Messages are delivered in pull mode, only	immediately after
-As XVC server access to FPGA	"lab-PC" is not close by.	destinations automatically.	delivering messages when requested.	pulling from servicebus.

Test Setup & Real-Time Debugging and Environment Monitoring & Data Management

- Test Setup: ESP32 with a sensor DTH11 is connected to a Kintex 7 FPGA through JTAG interface and is powered by the JTAG's VREF.
- Real-Time Debugging with XVC server.
- Environment Monitoring by distributing sensor data through Azure IoTHub and service bus queue.



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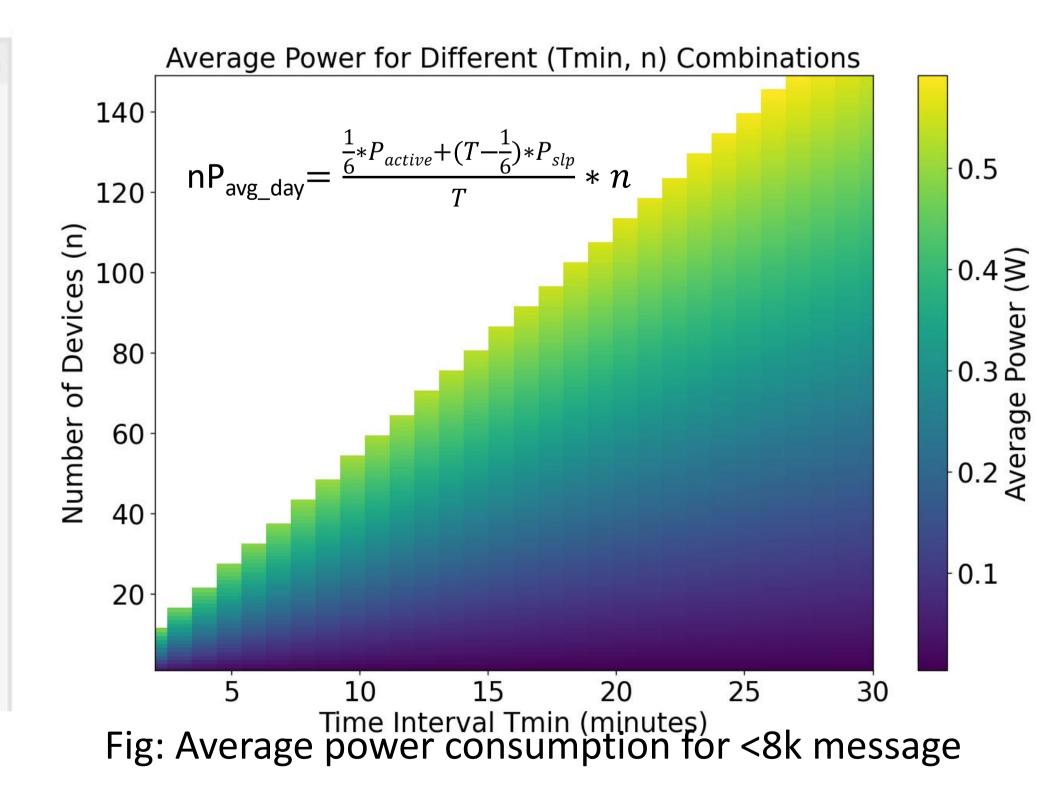


Fig: Setup for ESP32+Sensor+FPGA

Fig: Interface for FPGA debug

- Data Management and Quality Assurance:
 - Data from service bus queue is systematically written into a local database.
 - Successfully monitoring data during 42.8 hours continuous test period. There are 27 message loss, resulting in a data loss rate of 0.53%.
- Power consumption:
 - ESP32 works in XVC mode and sensor monitoring mode, in the latter mode, ESP32 switches periodically between normal operation and deepsleep.
 - The power with XVC run is 0.7W, the power for normal operation is 0.5W, the power with deepsleep is less than 1mW.
- Extra features:
 - Simultaneous Debugging of Multiple FPGAs.
 - Monitoring I2C sensors located on FPGA card via slighly modified JTAG connector pinout.