Real Time FFT Calculation Using FPGA PCIe Card for KSTAR Magnetohydrodynamic Analysis

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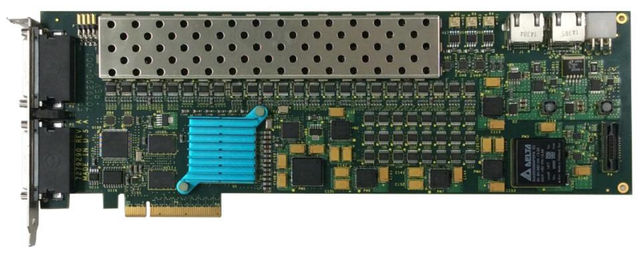
A real time data acquisition system is being implemented using a configurable multi-functional FPGA PCIe card. The FPGA card acquires 16 channels signal at 250 kHz, calculates 512-point Fast Fourier Transform (FFT), and provides the full data set of both original raw data and FFT derived data to the real-time computer. Data is recorded to the Korea Superconducting Tokamak Advanced Research (KSTAR) MDSplus database outside of plasma control system (PCS) for analysis and internal to PCS for algorithm use. Part of the real time version of disruption event characterization and forecasting (DECAF) running inside PCS uses this input for internal calculations.

When constructing the FFT engine in hardware, Intel FFT IP core is used to implement FFT. The detailed pipelining and timing for 16 channel 512 sample points for the FFT engine is described in the paper. Dual FIFO and RAM ping pong architecture are used for data reading, processing, and writing. The test result shows that the pipelined FFT engine works as expected.

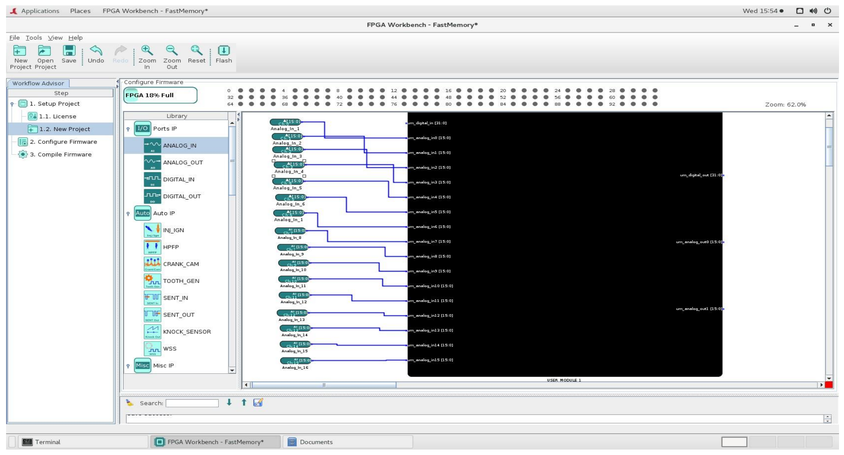
Arria V Programmable FPGA Card

Concurrent Real-Time's family of programmable FPGA PCIe cards is selected for this application. It uses Altera Arria V family FPGA with 504k logic elements. The cards can control up to 96 digital I/O signals along with 16 analog inputs (16-bit) and 16 analog outputs (16-bit). Each card's I/O functionality is fully customizable by the user by means of the FPGA Workbench tools.



FPGA Workbench

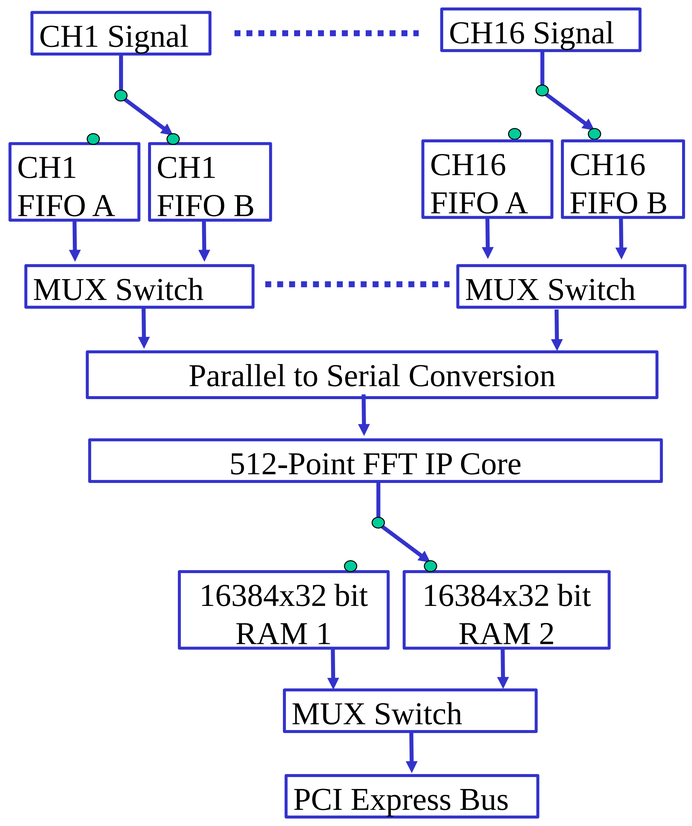
FPGA Workbench provides a complete development environment for building customized solutions based on Concurrent Real-Time's programmable FPGA cards. FPGA Workbench includes a powerful GUI for selecting and configuring a wide range of pre-developed data acquisition interface. FPGA Workbench is also needed to flash the firmware to the card through PCIe bus. The FPGA design software is Intel Quartus Prime Standard edition.



Here are the simulation result for 16 Channel FFT. Truncated sin wave signal with some noise and dc offset are applied only on odd number channels. The signal on the even number channels are zero.

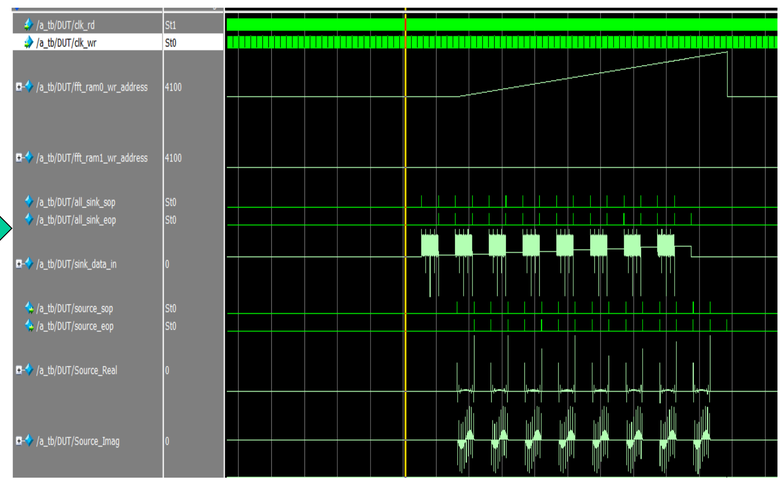
- sink_sop is the start of the 512 sampled data for each channel.
- sink_eop is the end of the 512 sampled data for each channel.
- sink_real is the input data from 16 channel.
- source_sop is the start of the 512 FFT calculation data for each channel.
- source_eop is the end of the 512 FFT calculation data for each channel.
- source_real is calculated FFT result real part.
- source_imag is calculated FFT result imaginary part.

Implementation FFT on Parallel Incoming Data using Intel FFT IP core

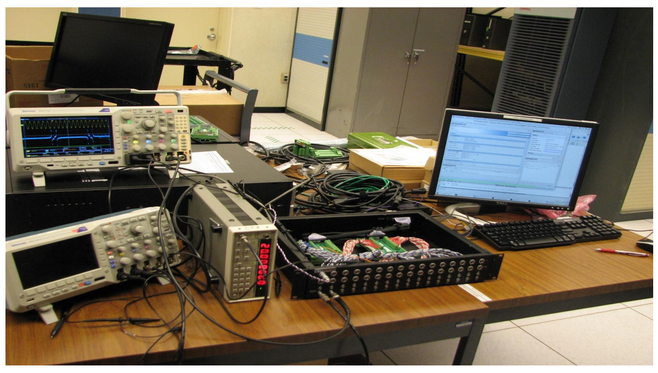


1. The sample rate for the input signal is 250 kHz. Two 1024x16 bit FIFO are used for each signal channel. Double clock FIFO is used. FIFO writing clock for the input data is 250 kHz. FIFO reading clock and the input clock for FFT IP core is 100MHz.
2. Ping-pong buffers (FIFO A and FIFO B) are used for each channel input data stream to avoid data loss. In the first buffer cycle, the data stream is buffered to FIFO A. When 512 samples are stored in FIFO A, the first buffer cycle ends. The stored data in FIFO A will be sent to FFT IP core for processing. At the same time, the second buffer cycle starts. The data stream is buffered to FIFO B. When 512 samples are stored in FIFO B, the second buffer cycle ends, and the first buffer cycle starts. The stored data in FIFO B will be sent to FFT IP core for processing.
3. To implement a single 512-point FFT on multiple channels combined, a 16 channel parallel data to a single channel serial data conversion unit is designed and implemented.
4. Intel FFT IP core is a high performance, highly-parameterizable FFT processor. to perform FFT calculations on the signals. The block-floating 512-point (16-bit) streaming FFT is selected to ensure the full use of the data width within the FFT function and throughout the transform.
5. Two ping-pong RAMs (16384 x 32 bit) are used to store the FFT results and the original raw data. There are three operation cycles for each RAM. In the first cycle, RAM accept the raw data from the FIFOs (Ch1-Ch16). In the second cycle, RAM accept the FFT calculation results. In the third cycle, the raw data and the FFT data are shifted to the PCI express bus and sent to the real time computer for process.

Modelsim Simulation Result



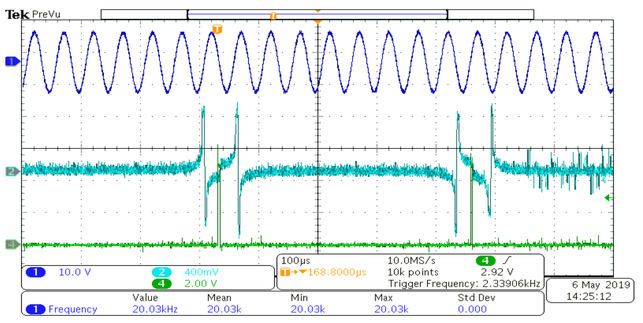
Single Channel FPGA FFT Verification Test Setup

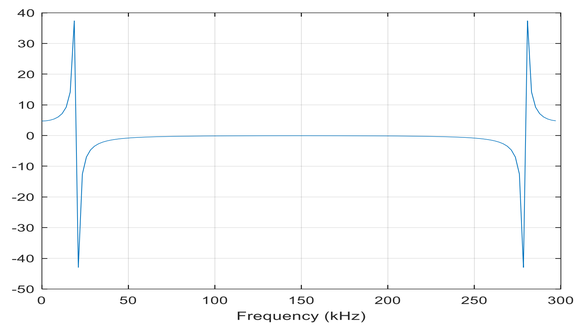


Computer is used to program the FPGA card and control the FPGA card. The black box is the chassis used as the interface between the FPGA card and the analog and digital (I/O) signals. Signal generator is used to generate the sin waveform input. Oscilloscope is used to monitor the input signal and the real-time FFT output signal.

FPGA Card Real part of FFT Test Results

Dark blue: 20 kHz sin wave input signal
Light blue: FPGA card FFT calculation result output through 16-bit D/A.
Green: Start point and End point FFT indicator

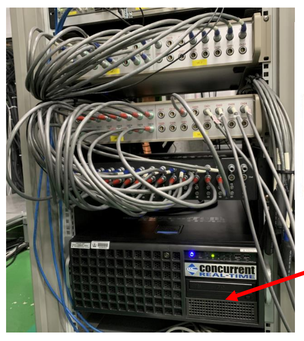




MATLAB Simulation Result

Real-time MHD System ON KSTAR

Real-time MHD instability measurement hardware to be used for disruption prediction and avoidance have been installed on the KSTAR.

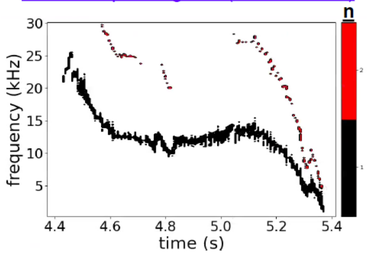


KSTAR buffer chassis (diagnostic interface box)

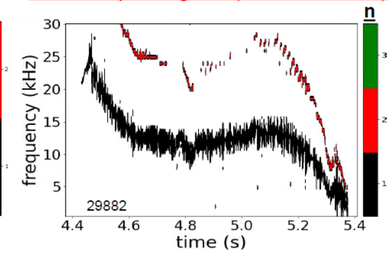
KSTAR real Time Computer

Real-time MHD system on KSTAR computed real-time FFTs from the toroidal magnetics probes for the first time in 2021 for real-time DECAF application.

DECAF spectrogram (offline FFTs)



DECAF spectrogram (real-time FFTs)



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