Real-Time Cross-Coupling removal and Monitoring in RF feedback systems: HLS-based FPGA implementation

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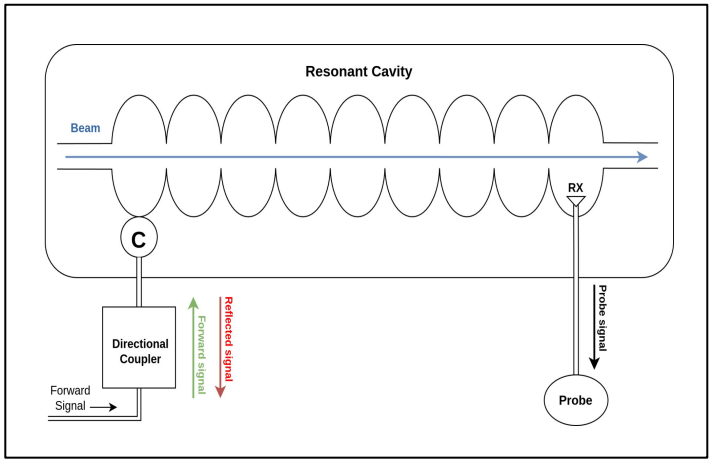
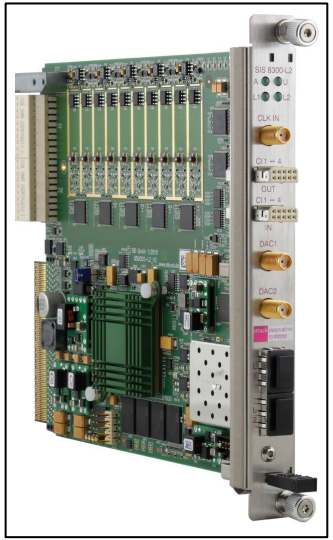
[1] Julien Branlard et al., "MTCA.4 LLRF System for the European XFEL", Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2013
[2] SIS8300-L2 MTCA.4 DIGITIZER (https://www.struck.de/sis8300-l2.html)
[3] AMD Vivado Design Suite (https://www.xilinx.com/products/design-tools/vivado.html)
[4] MicroTCA DAMC-TCK7 (https://innovation.desy.de/technologies/microtca/boards/damc_tck7/index_eng.html)
[5] Vitis High-Level Synthesis User Guide (UG1399)



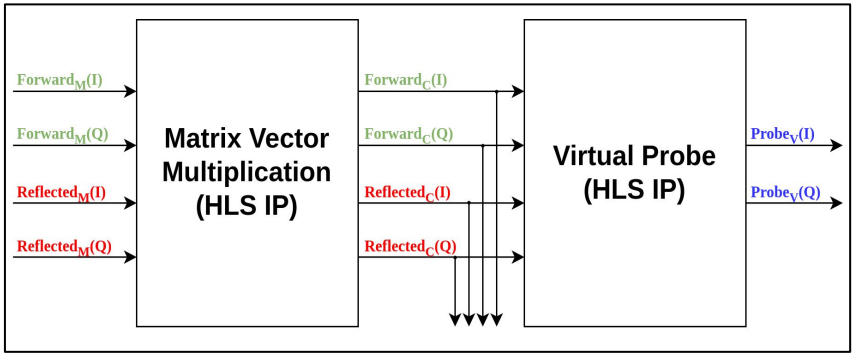
The structure of a single resonant cavity

In E-XFEL [1] we have **8 Cavities** within each of **4 Cryogenic Modules (CM)** => **32 I/Q** Forward and Reflected signals per CM

Sampling of **Forward** and **Reflected** signals are done by the SIS8300-L2 board



SIS8300-L2 digitizer MTCA [2]



This complex system needs a **cross-correction** entity that removes the Cross-Coupling of signals

HLS FPGA design for **cross-coupling removal & monitoring**

The results of FPGA implementation

Unroll factor	*Clock Period (ns)*	*Latency (ns)*	*DSP usage*
1 (HLS MVX)	6.1	**360**	**64**
4 (HLS MVX)	6.1	**213**	**256**
1 (HLS MVX)	12.2	**525**	**64**
4 (HLS MVX)	12.2	**232**	**256**
1 (HLS VP)	6.1	**140**	**8**
4 (HLS VP)	6.1	**67**	**32**
1 (HLS VP)	12.2	**281**	**8**
4 (HLS VP)	12.2	**134**	**32**

Performance vs Resource usage of HLS IPs on the targeted FPGA device (DAMC-TCK7) [3][4][5]

Challenges => HLS integration & analysis (CDC, memory and interface generation, etc.), System identification, algorithmic thinking, FPGA resources
On the other hand => Generate generic configurations, Easier and fast in the end user side, Cross-corrections in a few 100s of ns, Real-Time system