Real-Time Cross-Coupling removal and Monitoring in RF feedback systems: HLS-based FPGA implementation

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Abstract

Implementing digital signal processing (DSP) solutions on FPGAs is a challenging task that requires technical knowledge of the system and the functionality of algorithms. Using High-Level Synthesis (HLS) tools for handling DSP tasks accelerate the implementation process and reduce the development stage. Moreover, HLS solutions decrease FPGA verification time and provide flexibility for configuring design parameters with extensive iteration capabilities. In this paper, hardware accelerator units are introduced to correct the driven Radio Frequency (RF) signals in Low-Level RF (LLRF) multi-cavity controller systems. In RF stations, a portion of the injected signal into cavities is reflected due to the mismatch in the frequency of the forward signal and the resonance frequency of cavities. The presented design improves the forward signal in multi-cavity stations by real-time removal of the cross-coupling effect from the signal. This is achieved using the concepts of pipelining, parallelism, and the proper usage of FPGA resources for DSP calculation. Moreover, the paper introduces a real-time monitoring system for RF systems. Proposed units are used for detecting anomalies in the system by comparing the actual probe signal from each station with the virtual probe calculated based on the input signal. The main benefits of this solution are real-time calculation of corrected signals using DSP techniques and the introduction of an anomaly detector. Furthermore, this design reduces the workload from other parts of the system by off-loading the correction and monitoring of the RF cavities, leading to better performance of the overall system.

The structure of RF signals in RF cavities

The structure of Multi Cavities and Cryogenic Modules

- The multi-cavity LLRF control systems at E-XFEL drive a single klystron to feed up to **32** superconducting **RF cavities** [1], and it consists of **4** identical **Cryogenic Modules (CM).**
- High-power RF from the klystron is split into **2** waveguide branches before the second split to have separate branches per CM.
- Each waveguide arm per CM has **4** extensions split once more to feed each of the cavities.

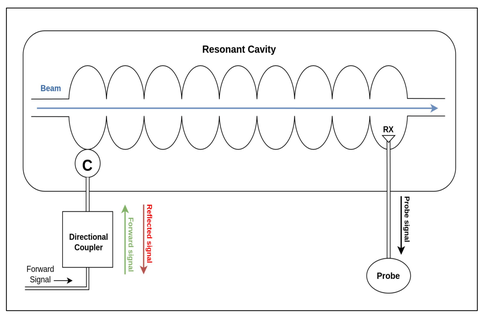

Figure 1) The structure of a single resonant cavity with 9-cells

- This paper focuses on the FPGA implementation of a **Real-Time cross-correction** entity that removes the Cross-Coupling of **Forward (F)** and **Reflected (R)** signals. Then another FPGA IP is introduced as a monitoring mechanism of the **Probe (P)** signal.
- The **Forward** signal refers to the propagated signal drive the cavity, the **Reflected** signal is the signal that gets reflected back due to impedance mismatches or other physical factors within the cavity. The **Probe** signal is intentionally introduced into the cavity for the feedback system in LLRF controller and it is also used for diagnostic purposes.
- In the case of E-XFEL, due to the limited isolation of the waveguide components and the RF measurement system, there are **cross-coupling** effects among the RF channels.

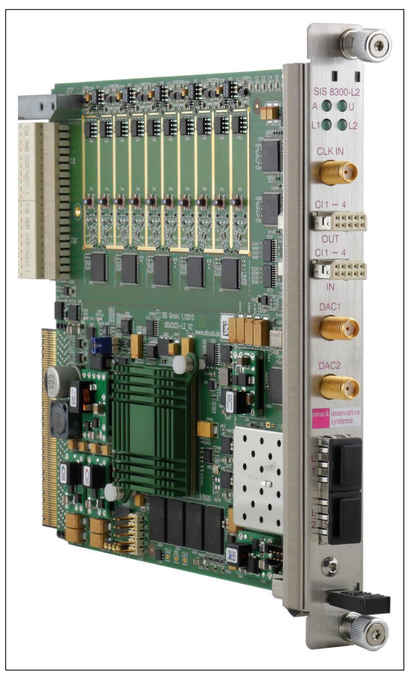

Figure 2) SIS8300-L2 digitizer MTCA

- To eliminate the effects of cross-coupling from each cavities, the **Matrix-Vector Multiplication (MVX)** FPGA IP is introduced.
- The second FPGA IP in this work is named as the **Virtual Probe (VP)** and it is responsible for calculating Probe values for cavities via the corrected Forward and Reflected signals from the previous stage.
- The feedback signals from the waveguide distribution system, i.e. Forward and Reflected signals associated with each cavity have a **natural coupling** among all, particularly between each other. The coupling among CMs is insignificant and negligible.
- Our solution provides the **decoupling** of the **8 Forward and Reflected** signal pairs that are sampled by the **SIS8300-L2** [2] boards. In the I/Q data formalism, this corresponds to decoupling of 32 digital signals. Therefore, our solution is capable to perform a **32 by 32** matrix multiplication of the measured signals.

[1] Julien Branlard et al., "MTCA.4 LLRF System for the European XFEL", Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2013

[2] SIS8300-L2 MTCA.4 DIGITIZER (https://www.struck.de/sis8300-l2.html)

Firmware implementation

The implementation of cross-coupling removal and monitoring system in FPGA

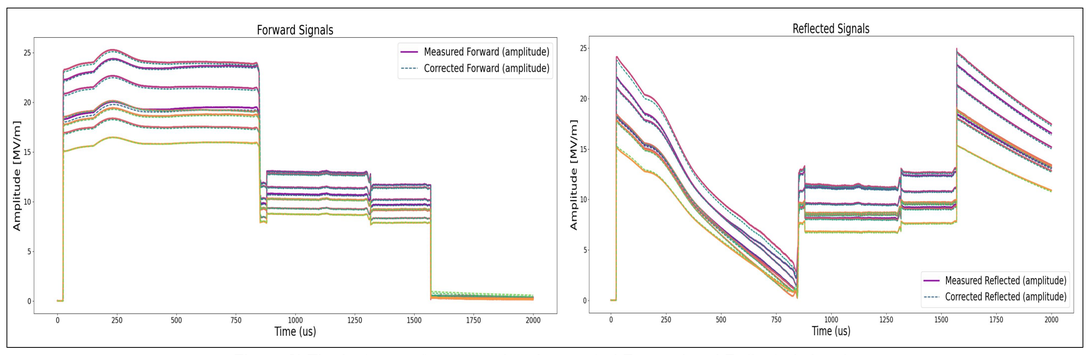

Figure 3) The instance of measured and corrected Forward and Reflected signals

- Inputs for the **MVX** are the measured **Forward and Reflected** signals, and the produced outputs are the **corrected values** of the equivalent signals for each cavity. The **coefficient values** are determined through a **system identification** process.
- The correction of input signals is achieved through the **parallel multiplication of the input vector** (Forward and Reflected signals) with a user-defined **coefficient matrix**. The computation is performed in **a few hundred of ns** in most of the configurations.
- Customized HLS **MVX and VP** IPs calculates corrected values for **8 cavities** by obtaining **8 pairs of I/Q** values for each **Forward and Reflected** signals.This instance requires a **coefficient matrix size of 32 by 32**. The corrected signals are feed into the **VP** IP and provides the **virtual Probe** signals.

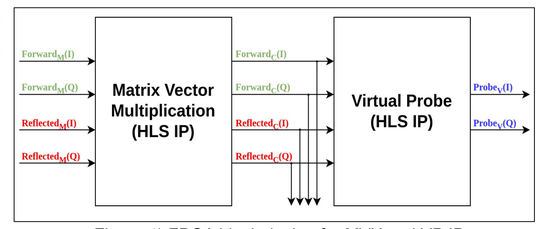

Figure 4) FPGA block design for MVX and VP IPs

- The following table shows the experimental results of **synthesizing MVX and VP** IPs using AMD Vitis HLS 2022 [3]. This experiment uses **Xilinx Kintex 7** [4] family (DAMC-TCK7 [5]).
- The design parameter **HLS unroll** [6] improves the performance of system by using more FPGA resources. It create N copies of the loop body and reduces the number of iterations.
- There are linear relations among **Unroll factor, Clock Period and DSP usage**. With considering the **maximum latency and FPGA resource**, a generic design is created.

32 by 32	*Unroll factor*	*Clock Period (ns)*	*Latency (ns)*	*Throughput (Clock Cycles)*	*DSP usage*	*FF usage*	*LUT usage*
HLS MVX	1	6.1	**360**	32	**64**	~21 K	~15 K
HLS MVX	2	6.1	**262**	16	**128**	~38 K	~27 K
HLS MVX	4	6.1	**213**	8	**256**	~75 K	~54 K
HLS MVX	1	12.2	**525**	32	**64**	~11 K	~12 K
HLS MVX	2	12.2	**329**	16	**128**	~17 K	~22 K
HLS MVX	4	12.2	**232**	8	**256**	~29 K	~41 K
HLS VP	1	6.1	**140**	16	**8**	~4 K	~5 K
HLS VP	2	6.1	**91**	8	**16**	~4 K	~5 K
HLS VP	4	6.1	**67**	4	**32**	~5 K	~6 K
HLS VP	1	12.2	**281**	16	**8**	~4 K	~5 K
HLS VP	2	12.2	**183**	8	**16**	~4 K	~5 K
HLS VP	4	12.2	**134**	4	**32**	~5 K	~6 K

Table 1) Performance vs Resource usage of HLS MVX and VP IPs on the targeted FPGA device

[3] AMD Vivado Design Suite (https://www.xilinx.com/products/design-tools/vivado.html)

[4] 7 Series FPGAs Data Sheet: Overview (DS180)

[5] MICROTCA DAMC-TCK7 (https://innovation.desy.de/technologies/microtca/boards/damc_tck7/index_eng.html)

[6] Vitis High-Level Synthesis User Guide (UG1399)

Physical origin of crosstalk

Board cross-talk / System identification

- MSK ADC boards sample **multiple RF signals in parallel** [7].
- Due to the finite RF isolation, the **ADC readings are affected by RF signals of other channels.**
- The measured RF cross-talk among channels can have **a magnitude up to -73.7 dB.**
- The cross-talk **can be measured in Real-Time using the Drift Compensation Module** [8].
- Then the channel decoupling **can be expressed with a complex matrix multiplication.**

[7] http://www.struck.de/sis8300-l2.html

[8] Ludwig et al., "Drift calibration for the European XFEL", LLRF Workshop 2017, Barcelona, Spain.

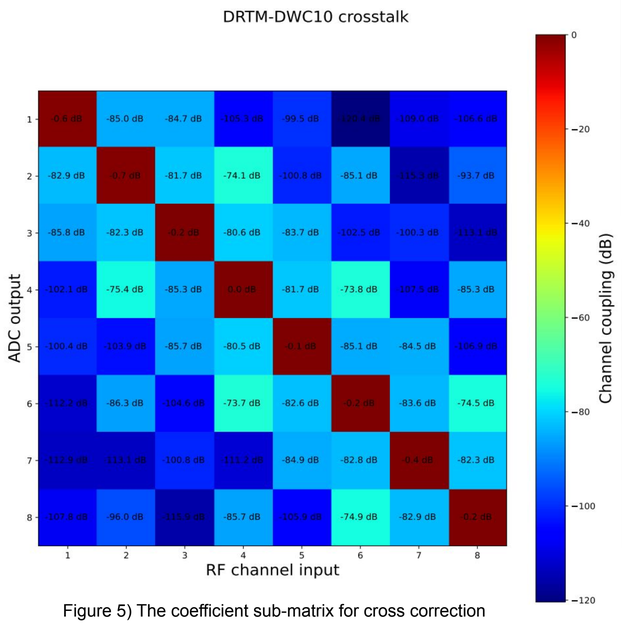

Figure 5) The coefficient sub-matrix for cross correction

Physical origin of crosstalk

Directional coupler cross-talk

- Forward and Reflected cavity signals are measured using **directional coupler placed on the RF waveguide.**
- Due to the final directivity of the couplers, the measured signal on both channels **is a linear combination of the Forward and Reflected** signals**.**
- By deriving the coupling parameters [9, 10], **it is possible to calculate the true Forward and Reflected** cavity signals in **Real-Time.**

[9] Pfeiffer, Sven, et al. "Virtual cavity probe generation using calibrated forward and reflected signals." MOPWA040, IPAC 15 (2015).

[10] Bellandi, A., Branlard, J., Diomede, M., Herrmann, M., Pfeiffer, S., & Schmidt, C. (2024). Calibration of superconducting radio-frequency cavity forward and reflected channels based on stored energy dynamics. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 169172.

Figure 6) *S.P.A. FERRITE, WDHC 3-3A bi-directional coupler for 1.3 GHz waveguides used at EuXFEL. The declared directivity is 40 dB. Courtesy of B. Yildirim and V. Katalev*

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HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

MSK. Maschine Strahlkontrollen

FWK FPGA firmware framework

European XFEL