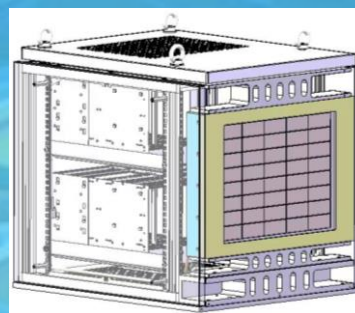


Design and Implementation of DAQ System for HEPS-BPIX4

XuanZheng Yang , Xiaolu Ji , Kejun Zhu , Shuihan Zhang

HEPS-BPIX4 6M detector

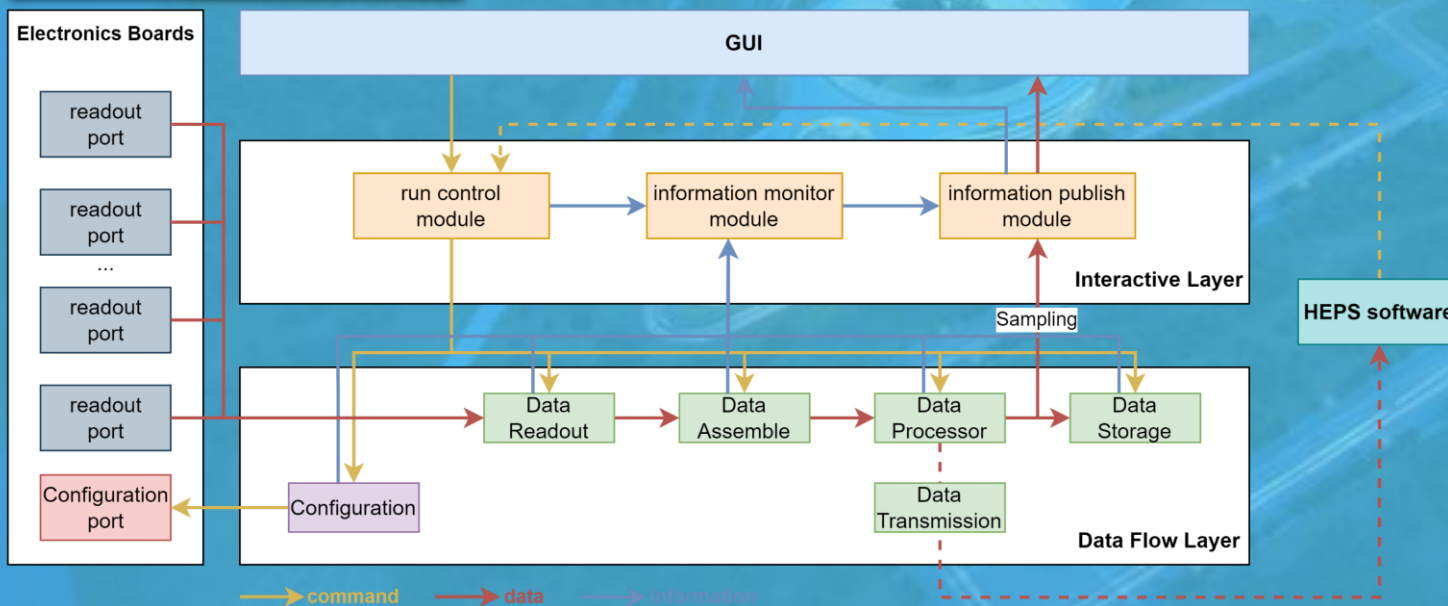
- a silicon pixel detector with 6 million pixels
- Designed for the High Energy Photon Sources (HEPS), China



HEPS-BPIX4 6M detector

Detector Parameters	Value
Module Number	40
Threshold	2
Pixel Number	6M
Max Counting Depth	16bit
Max Frame Rate	1kHz
Max Readout Bandwidth	192Gbps

Software Architecture



HEPS-BPIX4 DAQ System requirements

- large detection area
- high spatial resolution
- wide dynamic range
- high frame rate for data acquisition

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Introduction and Motivation

Framework Design And Implementation


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中国科学院高能物理研究所
Institute of High Energy Physics, Chinese Academy of Sciences

Design and Implementation of DAQ System for HEPS-BPIX4

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1. Introduction

- The HEPS-BPIX4 GM detector is a silicon pixel detector with 6 million pixels
- Designed for the High Energy Photon Source (HEPS), which is the first fourth-generation synchrotron light source in China
- The Data Acquisition (DAQ) System is an essential part of the detector system

Characteristics for HEPS-BPIX4 GM DAQ:

- Massive data readouts, reliable real-time data processing and storage
- Flexible system control → Support two modes:
 - Independent operation mode
 - Joint operation mode (transmitting data to HEPS software)
- High integration → Minimize nodes (target single server)

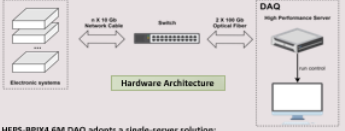


High performance requirements for HEPS-BPIX4 GM DAQ:

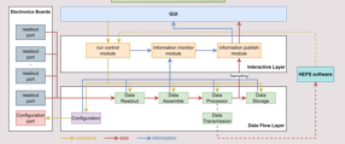
- large detection area
- high spatial resolution
- wide dynamic range
- high frame rate for data acquisition

Detector Parameters	Value
Detector Module Number	40
Threshold	2
Pixel Number	6M
Pixel Size	140μm × 140μm
Max Counting Depth	16bit
Max Frame Rate	15Hz
Max Readout Bandwidth	192Gbps

2. Architecture Design



HEPS-BPIX4 GM DAQ adopts a single-server solution: Considering the small volume of the silicon pixel detector, light-weight DAQ is easy to deploy and maintain flexibly for the entire machine



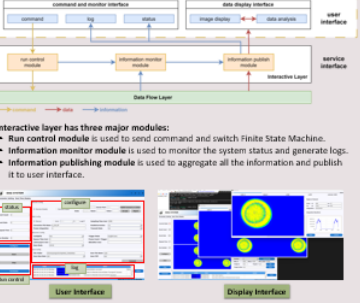
The DAQ system can be divided into two parts:

- Data flow layer** is responsible for data receiving, assembling, processing and saving
- Interactive layer** is designed for the control, monitoring, information publishing

Two layers are independent, TCP/IP is used to passing messages between them


Make full use of single-server resources to build a high-performance DAQ system

3. Framework Design



Interactive layer has three major modules:

- Run control module** is used to send command and switch Finite State Machine.
- Information monitor module** is used to monitor the system status and generate logs.
- Information publishing module** is used to aggregate all the information and publish it to user interface.



Dataflow Layer has four major components:

- RD:** Readout data from electronics readout boards → Using multi-threads
- EB:** Build data package based on the frame ID
- DP:** Implements data process functions and samples the data to the GUI interface.
- DS:** Save data to disk. Compression algorithms will be employed in the future to reduce storage bandwidth pressure

The core functionality of the HEPS-BPIX4 DAQ has been successfully implemented and tested with a single-detector module, validating its feasibility and reliability

4. Performance Study

The DAQ was deployed on the Dell PowerEdge R760 server to comprehensively evaluate the overall performance of the HEPS-BPIX4 GM DAQ system

Server	Dell PowerEdge R760
CPU	Intel(R) Xeon(R) Platinum 8422Y@2.80GHz
CPU(s)	2
Logical cores	128
Linux Kernel Version	4.18.0
Network Interface Card	100Gb
Hardware RAID	Dell PERC12

Raid	Raid5	Raid5 X 2	Raid0	Raid10
Block size	16K	16K	16K	16K
Threads	64	64	64	64
File Sequential Write	>10 GB/s	>20GB/s	~15GB/s	~9GB/s

- This configuration can meet the output bandwidth
- Compression algorithms will be employed to reduce storage bandwidth pressure

HEPS-BPIX4 Data Flow	
RCS	multi-threads readout ~10 CPU cores
EB	data assembly 2 CPU cores
DP	mapping transformation flat fielding ~20 CPU cores (w/o comp)
DS	pixel calibration real-time storage ~30 CPU cores

Estimation for the resources required

Preliminary confirm the feasibility of the HEPS-BPIX4 GM DAQ

5. Conclusion

The single-server HEPS-BPIX4 GM DAQ system offers fundamental features including data transfer, configuration, display, and data storage. It will be officially deployed in the HEPS light source beamline system this year.

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Architecture Design

Conclusion

- ✓ DAQ core functionality fully implemented
- ✓ Applied in single-detector module calibration
- ✓ comprehensively evaluate overall performance
- ✓ will be deployed this year

Performance Study

Welcome to discuss
Session : post B (#131)