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A new methodology of clock phase adjustment in a large-scale clock distribution system for HL-LHC ATLAS TGC front-end electronics

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Accurate clock distribution to front-end electronics is crucial in optimizing physics performance in collider experiments, especially for triggering applications. In the ATLAS detector, the Thin Gap Chamber (TGC) system performs fast online muon reconstruction using a coincidence algorithm as part of the first hardware-based triggering stage. Preparing for the High Luminosity LHC (HL-LHC), an upgrade to the entire TGC trigger and readout electronics system for the ATLAS experiment is planned (Phase-2 upgrade). During the initial stages of trigger and readout, electronics conduct precise assignment of individual rising edges of binary hits from the TGC chambers to specific bunch crossings. Here, clock phase adjustment plays a vital role in maximizing correct identification performance. This process involves 1,434 frontend electronics, with clock signals distributed via 1,434 optical fibers and reconstructed individually in the Phase-2 TGC system. For effective bunch-crossing identification in TGC trigger electronics, clock tuning well below O(1) ns is necessary. We've developed a methodology for measuring the clock phase for individual reconstructed signals across the entire system comprising 1,434 frontend modules and aligning the phase remotely and automatically in situ. Two custom VME modules were designed for this purpose, thoroughly tested, and proven to be fully functional. This presentation presents a methodology developed to ensure low-skew clock signal distribution, focusing on efforts to maintain aligned clock signals across the large-scale electronics system. A measurement-driven estimation of the expected size of skew to be absorbed and the expected uncertainties on the alignment will also be discussed.

Minioral

Yes

IEEE Member

No

Are you a student?

No

Author: HORII, Yasuyuki (Nagoya University (JP))

Presenter: Mr NAGASAKA, Ren (University of Tokyo (JP))

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