A new methodology of clock phase adjustment in a large-scale clock distribution system for HL-LHC ATLAS TGC front-end electronics

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***Abstract*—Accurate clock distribution to front-end electronics is crucial in optimizing physics performance in collider experiments, especially for triggering applications. In the ATLAS detector, the Thin Gap Chamber (TGC) system performs fast online muon reconstruction using a coincidence algorithm as part of the first hardware-based triggering stage. Preparing for the High Luminosity LHC (HL-LHC), an upgrade to the entire TGC trigger and readout electronics system for the ATLAS experiment is planned (Phase-2 upgrade). During the initial stages of trigger and readout, electronics conducts precise assignment of individual rising edges of hit signals from the TGC chambers to specific bunch crossings. Here, clock phase adjustment plays a vital role in maximizing trigger performance. This process involves 1,434 front-end electronics, with clock signals distributed via 1,434 optical fibers and reconstructed individually. For effective bunch-crossing identification in TGC trigger electronics, clock tuning well below O(1) ns is necessary. We have developed a methodology for measuring the clock phase for individually reconstructed clock signals across the entire system and aligning the phase remotely and automatically in situ. Two custom VME modules were designed for this purpose, thoroughly tested, and proven to be fully functional. This presentation presents a methodology developed to ensure low-skew clock signal distribution, focusing on efforts to maintain aligned clock signals across the large-scale electronics system. A measurement-driven estimation of the expected size of skew to be absorbed and the expected uncertainties on the alignment are also discussed.**

***Index Terms*—LHC, HL-LHC, ATLAS, TGC, DAQ, clock distribution, clock phase adjustment, FPGA, SoC**

I. The TGC electronics system for the HL-LHC ATLAS experiment

THE Large Hadron Collider (LHC) at CERN will be upgraded, and a peak instantaneous luminosity will be delivered up to 7.5×10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$ for the High-Luminosity LHC (HL-LHC) [1]. The corresponding number of pileup collisions per bunch crossing will reach 200. To collect events to search for physics of interest efficiently in this high luminosity environment, an upgrade of the ATLAS detector and trigger DAQ system, denoted as the Phase-2 upgrade, is foreseen.

The Thin Gap Chamber (TGC) detector [2] is used for the muon trigger system in the end-cap regions of the ATLAS detector. TGC is located in both endcaps of the ATLAS detector. Each side is divided into 12 independent sectors called 1/12 sectors in terms of infrastructure and operation.

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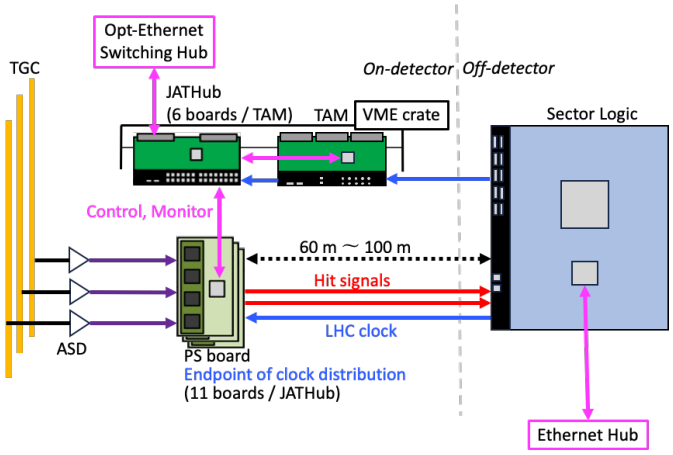

Fig. 1. The block diagram of the TGC electronics [3].

TGC is a multi-wire proportional chamber operated in a limited proportional mode. Signals from the anode wires and the strips, arranged in orthogonal directions, provide two-dimensional position measurements. Block diagram of the TGC electronics for the Phase-II upgrade is shown in Fig. 1. TGC signals are amplified and discriminated by the amplifier-shaper-discriminator (ASD) boards and fed into the PS board (front-end board). The Patch-Panel ASICs (PP-ASICs) on the PS board align the timing of the hits compensating for the difference in cable length and time of flight. After the arrival timing alignment, with reference to the LHC bunch clock synchronized with the LHC bunch crossing at 40 MHz, each rising edge of signals is assigned to bunch crossings, which is called the bunch crossing identification (BCID). A PS board transmits the hit bitmap data of 256 channels (fixed length) to the Sector Logic by two optical fibers, each of which manages the transfer rate of 8 Gbps. In addition to data transmission, the PS board receives timing signals synchronized to the LHC clock from Sector Logic by optical fiber. The FPGA on the PS board controls the timing parameters of the PP-ASICs and the ASD discriminator threshold. PS board is the endpoint of the clock distribution in the TGC system.

Muon tracks are reconstructed by a pattern recognition algorithm using the coincidence of TGC layers for every bunch crossing on Sector Logic, based on the TGC hit BCID. To maximize the performance of the hit BCID, low-skew

clock distributions to the front-end PS boards are essential. Sub-nanosecond timing precision, inclusive of timing arrival control and clock distribution, is known to be the target to realize the good performance of the TGC hit BCID. The distributed and reconstructed clock signals on the individual 1,434 PS boards need to be well controlled within sub-nanosecond precision.

Two custom VME modules, JTAG Assistance Hub (JATHub) and Timing Alignment Master (TAM), have been designed for this purpose. JATHub and TAM are designed around an AMD Zynq-7000 and an AMD Kintex-7 device, respectively. JATHub measures the phase of the clock reconstructed by the PS board. The clock phase measurement with the JATHub is conducted with respect to the reference clock signals reconstructed and distributed by TAM, which receives the signals from Sector Logic via optical fiber using the same methodology as the clock distributions to PS boards.

II. The Methodology of Clock Phase Adjustment

THE overview of the clock phase adjustment methodology is shown in Fig. 2. The concept of clock phase adjustment is to measure clock phase at the endpoints (PS boards) and adjust the clock phase individually on PS boards. We have developed a methodology of clock phase measurement and adjustment of all 1,434 PS boards remotely in a semi-automated manner by introducing the JATHubs and TAMs. The procedures of clock phase adjustment are as follows:

1) Sector Logic distributes timing signals including the LHC clock to PS boards and TAMs.
2) Phase of recovered clocks on all 26 individual TAMs is aligned (green line).
3) TAM distributes reference clock for six JATHub with a low skew (blue line).
4) A JATHub can measure eleven PS boards at maximum, and a JATHub measures the relative clock phase of PS boards with respect to the reference clock distributed from TAM (red line).
5) Optimal clock variable delay on PS boards is determined based on the measurement and adjusted.

Item 2 is called “clock phase adjustment among 1/12 sectors”. Items 3 and 4 are called “clock phase adjustment within 1/12 sector”.

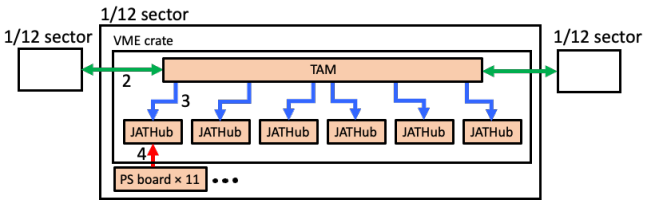

Fig. 2. Overview of the clock phase adjustment methodology.

III. Implementation of Key Functionalities in FPGAs and SoCs

THREE key functionalities are designed and implemented for the clock phase adjustment, which are (A) clock distribution and reconstruction with fixed latency, (B) variable phase shift (coarse and fine delay), and (C) clock phase measurement.

A. Clock distribution and reconstruction with fixed latency

Data and timing signals are serialized with 8b/10b encoding and sent to the front-end boards (PS boards and TAMs). PS boards and TAMs decode and reconstruct clock information without phase ambiguity, denoted as “fixed latency” We have established dedicated implementation techniques to realize clock recovery without phase ambiguity shown in Fig. 3.

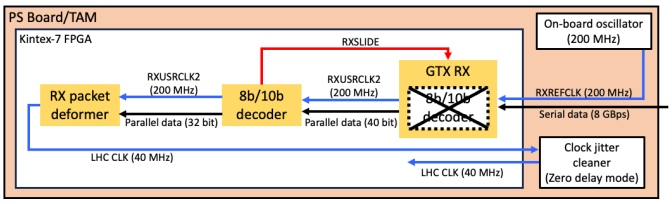

Fig. 3. Implementation of clock distribution with fixed latency. The data shifts right by one bit for every RXSLIDE (red line) pulse issued. The 8b/10b decoder decodes 40-bit data to 32-bit data by assigning RXSLIDE unless comma word is detected. The RX packet deformer reconstructs 40 MHz clock from 200 MHz clock with fixed latency using header word defined in data format.

B. Variable phase shift (coarse and fine delay)

Variable coarse and fine delay functionalities are implemented. The coarse delay has a 25 ns step and is implemented as a shift register with BRAM [4]. The fine delay has 1/56 ns ($\approx$ 18 ps) step and is implemented with phase shift functionality of the Mixed-Mode Clock Manager (MMCM) [5].

C. Clock phase measurement

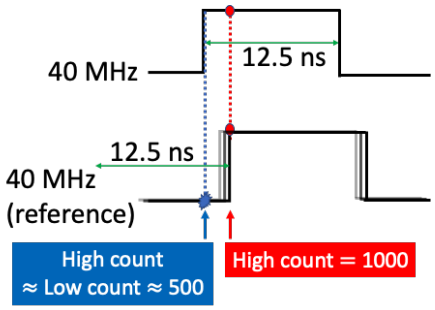

Fig. 4. Principle of clock phase measurement. The clock phase measurement procedures are as follows: 1. Sample the clock 1000 times at the reference clock phase. Measure the fraction of high counts among the 1000 samples. 2. Shift the phase of the reference clock by one step. 3. Scan for one unit interval (UI) of the clock.

The clock phase measurement method is implemented in JATHub and TAM. TAM uses the functionality to align the reference clock among all TAM. JATHub exploits the feature

to measure the relative clock phase of all the belonging PS boards.

The concept of actual implementation of the clock phase measurement is shown in Fig. 4. The clock phase measurement procedures are as follows:

1) Sample the clock 1000 times at the reference clock phase. Measure the fraction of high counts among the 1000 samples.
2) Shift phase of reference clock by one step.
3) Repeat and scan for one unit interval (UI) of the clock. We use 40 MHz clock with one UI of 25 ns for determining fine delay parameters and 200 kHz clock with one UI of 5 us for coarse delay parameters.

IV. Demonstration of the Clock Phase Adjustment among 1/12 Sectors

THE demonstration of the clock phase adjustment among 1/12 sectors has been made with two TAMs.

A. Setup

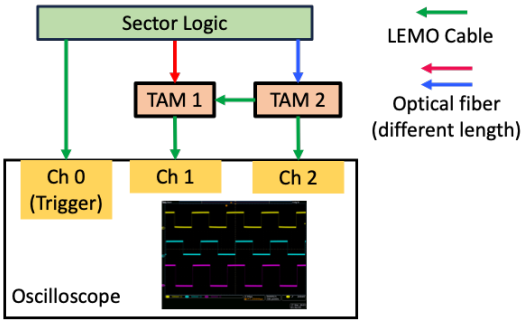

Fig. 5. Setup of the demonstration of clock phase adjustment between 1/12 sectors. Sector Logic distributes the clock to two TAMs via optical fiber. The LEMO cables are aligned aiming for TAM 2 to match its clock phase to TAM 1.

Fig. 5 illustrates the demonstration setup for the two TAMs. This configuration enables us to perform phase adjustments between the two TAMs to provide an aligned reference clock to the JATHubs. The Sector Logic distributes clock signals to two TAMs (TAM 1 and TAM 2 in the figure) with varying fiber lengths for demonstration purposes. TAM 1 then compares the recovered clock phase difference between itself and TAM 2. The coarse delay and fine delay parameters required to align the clock phase between two TAMs are calculated. We have implemented the software tools and the relevant firmware to ensure that the procedure can be completed automatically and remotely.

B. Result

Fig. 6 displays the demonstration results. Following the procedure, the clock phases of the recovered clocks on TAM 1 and TAM 2 are well aligned with an accuracy of about 100 ps.

This confirms the clock phase adjustment accuracy between the two TAMs in distributing a phase-aligned reference clock

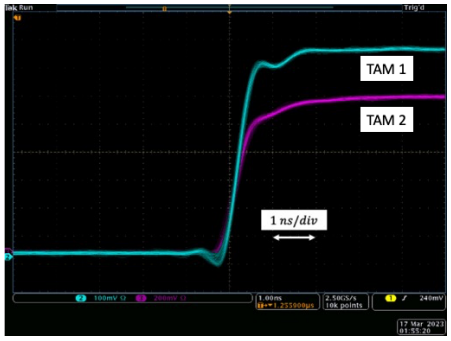

Fig. 6. Result of the demonstration of clock phase adjustment between 1/12 sectors. one division is set to 1 ns. The clock phase of TAM 2 matches TAM 1 with sufficient accuracy. The clock pulse heights of two TAMs are changed for ease of viewing.

for future clock phase measurements at JATHub. The procedure for "clock phase adjustment among 1/12 sectors" will involve a sequence of clock phase adjustments between two TAMs (refer to Fig. 2). Since scaling up from this setup to the full system should be straightforward, the demonstration validates the methodology of the "clock phase adjustment among 1/12 sectors" for the full system.

V. Demonstration of the Clock Phase Adjustment within 1/12 Sector

THE clock phase adjustment within 1/12 sector is demonstrated and explained in this section.

A. Setup

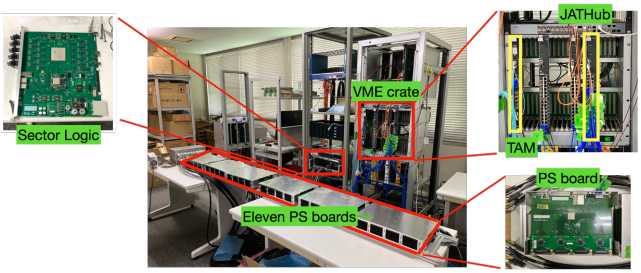

Fig. 7. Picture of the demonstration of clock phase adjustment within 1/12 sector.

Fig. 7 and Fig. 8 illustrate the demonstration setup for the eleven PS boards, JATHub, TAM, and Sector Logic. This configuration enables us to perform phase adjustments between the eleven PS boards. The Sector Logic distributes clock signals to eleven PS boards with varying fiber lengths for demonstration purposes. JATHub then measures the phase of the clock signals reconstructed on the individual PS board with respect to a reference clock distributed from TAM. The coarse delay and fine delay parameters required to align the clock phase between eleven PS boards are obtained. We have implemented the software tools and the relevant firmware to ensure that the procedure can be completed automatically and remotely.

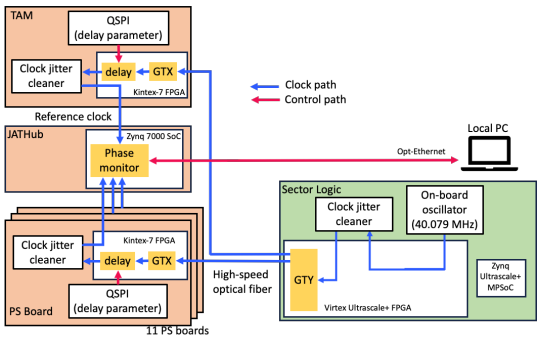

Fig. 8. Schematic view of the demonstration of clock phase adjustment within 1/12 sector. Sector Logic distributes the clock to 11 PS boards and TAM via optical fiber. TAM distributes reference clock to JATHub. JATHub monitors the clock phase of 11 PS boards. Results of clock phase measurement are obtained via ethernet. Sector Logic rewrites optimal delay parameters of 11 PS boards.

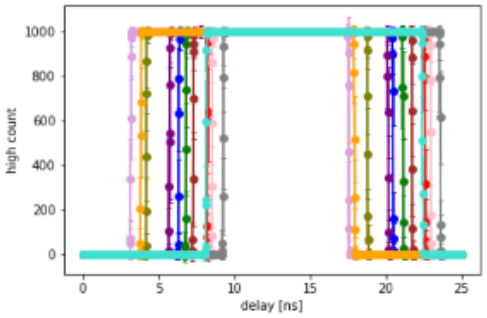

Fig. 9. The high count (see Fig. 3) depending on the delay before the demonstration of clock phase adjustment within 1/12 sector (25 ns window).

B. Result

Fig. 9 displays the high count (see Fig. 3) depending on the delay before the demonstration. Fig. 10 and Fig. 11 display the demonstration results. Following the procedure, the clock phases of the recovered clocks on eleven PS boards are well aligned with an accuracy of ~ 50 ps. The ~ 50 ps uncertainty arises from remaining phase irreproducibility with transceiver reset (details in Sec VI). This confirms the clock phase adjustment methodology within 1/12 sector. Since scaling up from this setup to the full system should be straightforward, the demonstration validates the methodology of the "clock phase adjustment within 1/12 sector" for the full system.

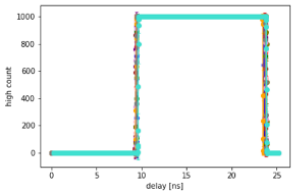

Fig. 10. Results of the demonstration of clock phase adjustment within 1/12 sector (25 ns window).

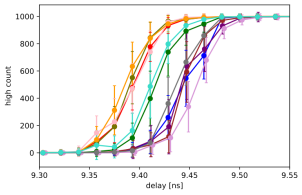

Fig. 11. Results of the demonstration of clock phase adjustment within 1/12 sector (zoom-in window).

VI. Reproducibility and Part-to-Part Skew

We have carefully checked reproducibility and part-to-part skew. The primary sources of phase measurement uncertainties are identified as stemming from the measurement's reproducibility and the part-to-part skew of components involved in clock phase measurements.

A. Reproducibility

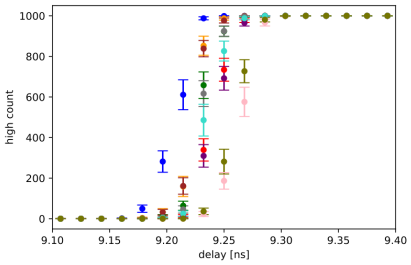

Fig. 12. Reproducibility of clock phase of a PS board. Each color corresponds to plots with all modules' reset steps.

To assess reproducibility, we repeated the clock phase adjustment procedure with power cycles. Fig. 12 illustrates the reproducibility of clock phase measurements of the PS board reconstructed clock. We noted a ~ 50 ps ambiguity in the phase measurement, attributed to phase irreproducibility in the current implementation around the transceivers, which suffices for our purpose of the ATLAS TGC system.

B. Part-to-part skew

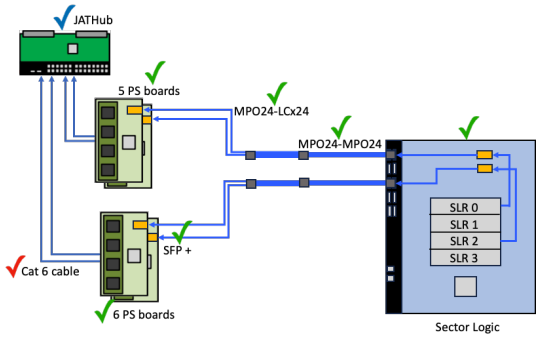

Fig. 13. Shematic view of the setup for the clock phase adjustment. The green check marks represent (1) part-to-part skew in the clock distribution system. The red and blue check marks represent (2) part-to-part skew in the clock phase measurement system, especially, red check marks represent part-to-part skew regarded as systematic uncertainty in our system.

We conducted measurements of the part-to-part skew of major components engaged in clock distributions and clock phase measurements. The results are summarized in Fig. 13 and 14. The skew is categorized into two types: (1) part-to-part skew in the clock distribution system, and (2) part-to-part skew in the clock phase measurement system. Identifying individual part skew involved in clock phase measurement enables us to

component	max [ns]	typical [ns]
SL port (same SLR)	1.5	0.7
SL port (different SLR)	3	1.5
MPO24-MPO24 (1 m)	0.2	0.1
MPO24-LC24 (1 m-1 m)	<0.01	-
SFP+ (same type)	<0.01	-
SFP+ (different type)	0.1	0.1
PS board	0.1	0.1
Cat 6 cable (10 m)	0.6	0.4
JATHub (LVDS receiver)	0.4	0.2

Fig. 14. Skew of each component related to clock phase adjustment. The green check marks represent (1) part-to-part skew in the clock distribution system. The red and blue check marks represent (2) part-to-part skew in the clock phase measurement system, especially, red check marks represent part-to-part skew regarded as systematic uncertainty in our system.

minimize uncertainties in the measurements, and we intend to measure part skew wherever feasible.

The skew of Cat 6 cables and LVDS receivers of JATHubs impacts clock phase measurements (Fig. 14). While we plan to measure the skew of all LVDS receivers of JATHubs, testing Cat 6 cables, already in use in the current working system for ongoing LHC runs and intended for the HL-LHC system, poses challenges, corresponding to uncertainties $\sim$ 600 ps. If we could eliminate part-to-part skew in the Cat 6 cables, we could reduce uncertainties to $\sim$ 50 ps, representing the ultimate performance of the method established in this study.

VII. Conclusion

In the ATLAS experiment at the HL-LHC, the TGC system involves a large number of front-end electronics (1,434) with timing signals distributed via optical fibers and reconstructed, individually. Effective bunch-crossing identification in TGC trigger electronics requires clock tuning well below O(1) ns. A methodology has been developed for measuring the clock phase for individual reconstructed signals across the entire system and aligning the clock phase remotely and automatically in situ. The reproducibility of fixed latency clock distribution is accuracy of $\sim$ 50 ps. All systematic skew observed by clock phase adjustment or taken into account when clock phase measurement are checked with the measurement-driven method. We can conclude that clock phase adjustment of 1,434 front-end electronics can be done with an accuracy of $\sim$ 700 ps ($=\sim$ 600 ps: skew of Cat 6 cable + $\sim$ 50 ps: uncertainty of reproducibility) which is sufficient for our requirement.

Acknowledgment

I would like to thank my supervisor, Dr. Yasuyuki Okumura, for his thoughtful guidance and technical assistance. This work was supported by JST SPRING, Grant Number JPMJSP2108.

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