A new methodology of clock phase adjustment in a large-scale clock distribution system for HL-LHC ATLAS TGC front-end electronics

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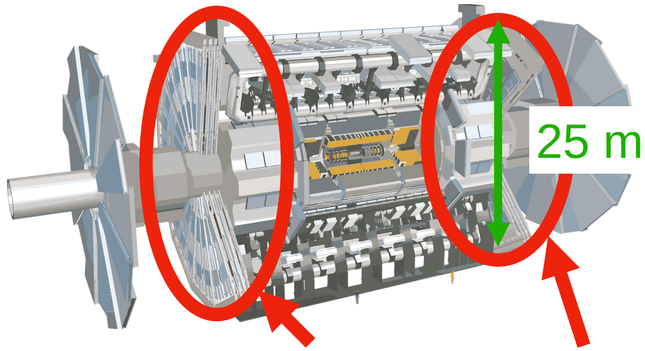
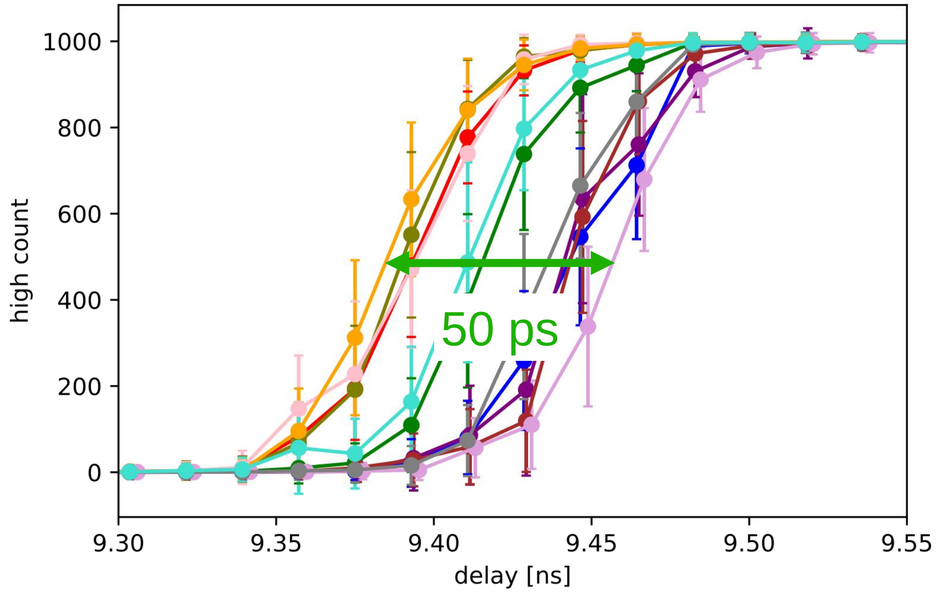
Key topic

- Methodology of clock phase adjustment for large-scale electronics system.
  - ATLAS Thin Gap Chamber system:
    - 1,434 front-end electronics.
    - 1,434 fibers to distribute clock signals for synchronization.
  - Requirement on clock phase adjustment:
    - Well better than 1 ns precision to guarantee good performance of hit-bunch crossing assignment (BCID), regarding 25 ns bunch spacing of LHC.
      - Note: 1 ns also corresponds to precision of signal arrival timing alignment.
      - Aim to O(100) ps.



Thin Gap Chamber

- Actual implementation of clock phase adjustment functionality in firmware and software.
  - Taking advantage of SoC devices, measurement, and adjustment of clock phase can be done remotely in a semi-automated manner.
- Validation of the system and estimation of the precision of the system.
  - Reproducibility validation
  - Estimation of uncertainty with measurement-driven method.



We conclude that phase adjustment of 1.434 front-end electronics can be done with an accuracy of ~ 50 ps (sufficient accuracy for our purpose).