Multi-port Remote JTAG over Optical Fibers under Radiation Environment

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Abstract —
JTAG protocol is a popular method to program FPGA devices where a more intelligent technology is not applicable. However, the original JTAG protocol is designed for a short distance connection and not necessarily suitable when the FPGA device is located in a remote radiation area. We developed a custom optical transmission technique for the JTAG protocol based on discrete devices, and implemented in a small test board receiver and a multiport JTAG distributor. We present the evaluation results and future applications.

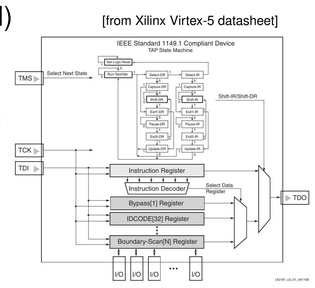
1. Introduction

JTAG protocol is heavily used in high energy physics, including the Belle II experiment at the SuperKEKB e^+e^- collider in Tsukuba, Japan.

JTAG

- Low-level protocol to access device via 3 input (TCK, TMS, TDI) and 1 output (TDO), driven by a state machine
- Most popular method to program FPGAs and debug firmware
- Designed for short distance, single-ended lines for single chain
- Multiple devices in a serial chain of TDO to TDI
- Tool are provided (e.g., Xilinx impact, chipscope, vivado)

[from Xilinx Virtex-5 datasheet]



Simple Extensions

- Longer distance by converting into LVDS
- Multiple devices can be programmed by multiple copies of input, and TDO output is expected to be identical for all target if there is no error

Problems

(1) TDI input to TDO output latency has to be within fixed TCK interval

(2) Not AC-balanced, simple conversion to optical lines is not possible with typical AC-coupled optical transceivers

⇨ **A new solution to overcome these two problems.**

2. JTAG at Belle II

Belle II detector consists of seven subdetectors, of which three of them are read out by the front-end electronics (FEE) boards located inside the detector.

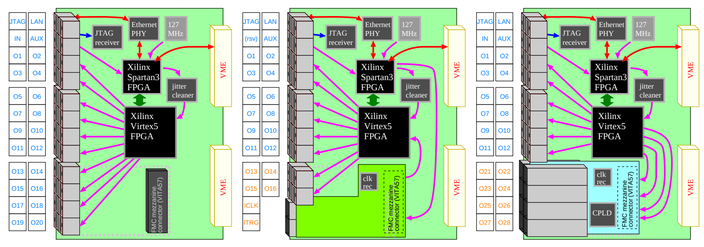
Remote JTAG targets at Belle II

- **CDC** (Central Drift Chamber) — 299 FEEs, with Xilinx Virtex 5
- **TOP** (Time-of-Propagation Counter) — 64 FEEs, with Xilinx ZYNQ
- **ARICH** (Aerogel Ring-Image Cherenkov Counter) — 72 FEEs, with Xilinx Virtex 5

Implementation

- **Receiver on a FEE** — LVDS signal translated to/from LVTTL/LVCMOS
- **Connection to FEEs** — LVDS over CAT7 cables of up to 15m
- **Distribution to FEEs** — up to 10 FEEs from one FTSW module (simultaneous parallel JTAG programming of the same-type device / same cable length)
- **Distribution to FTSWs** — over custom **b2tt** protocol as a part of timing-distribution
- **JTAG source** — custom **jtagft** program to perform typical programming sequences: initialize chain, get idcode, program, verify from a VME CPU + FTSW (no Xilinx apps)
- (optional for TOP — JTAG from Xilinx apps + programming cable converted into LVDS and routing was controlled by FTSW)

FTSW modules (3 variations)



3. Optical JTAG Design

Goal

- JTAG programming over optical fibers (optical modules are AC-coupled)

Requirements

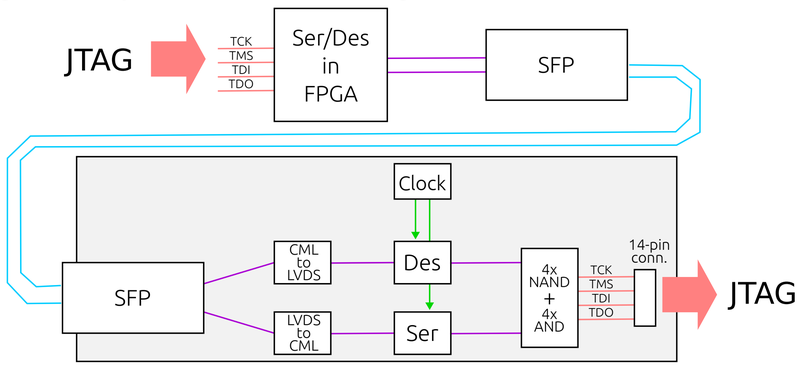
- Encode TCK/TMS/TDI and TDO signals into an AC-balanced signal
- Remote-end decoder/encode should not be a programmable device
- Up to ∼10 MHz JTAG signal is enough, no need of high-speed link

Device choice (non-programmable discrete chips only)

- Simple 12-bit Ser/Des (DS92LV1023 / DS92LV1224)
- On-board reference clock of the same frequency is needed
- 74-series AND/NAND gates (+ supervisor chip BD46272G) for LOCK detection

Belle II specific choices

- JTAG distributor is implemented in the FTSW module for **flexibility** and straightforward **multi-port extensions** up to 8 SFP transceivers from general I/O pins
- From 127.2 MHz system clock, Ser/Des rate is chosen to be 381.6 MHz: JTAG signals every 31.8 MHz and user logic at 190.8 MHz inside Virtex 5 of FTSW



[Similar optical JTAG design is already reported by B. Deng et al 2015 JINST 10 C01050 for ATLAS LAr system]

4. Evaluation with a Test Board

Test boards

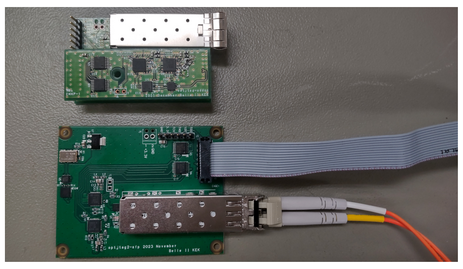
- Two types of prototype boards were produced
- Entire circuit fits within 2cm × 5cm area

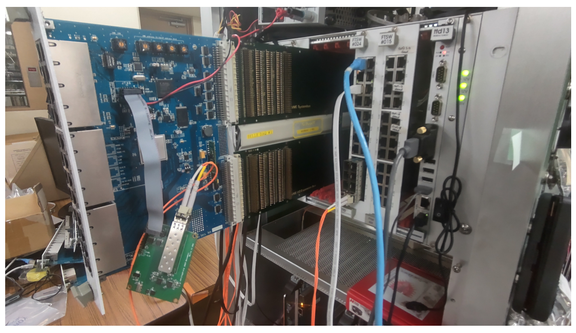
Test results

- Local-end implemented in the FTSW module / Target FPGA is another FTSW
- Minor issue 1: CML output of SFP cannot stably drive LVDS input of deserializer — need a CML to LVDS buffer
- Minor issue 2: deserializer's lock signal is not reliable when the SFP input is open — solved by adding a supervisor chip to wait for a stable lock signal
- JTAG operation confirmed, but only at 1.5 MHz due to the Ser/Des protocol overhead

Radiation tolerance

- Irradiated up to 2kGy of ^{60}Co γ-ray source with no loss of the functionality (sufficient for Belle II upgrade)

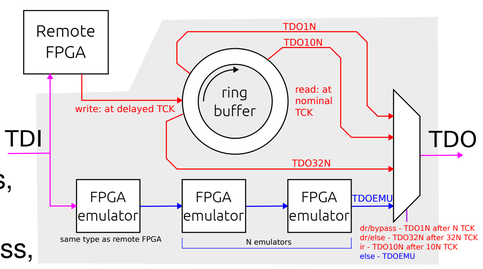




5. Overcoming the JTAG latency

Longer JTAG chain

- TDO has to be received within **one** TCK interval (∼160 ns for 6 MHz) for **one** FPGA, but can be within ***N*** TCK for ***N*** FPGAs in the chain
- FPGA emulators in the chain can absorb latency, if TDO of the target FPGA can be properly bypassed

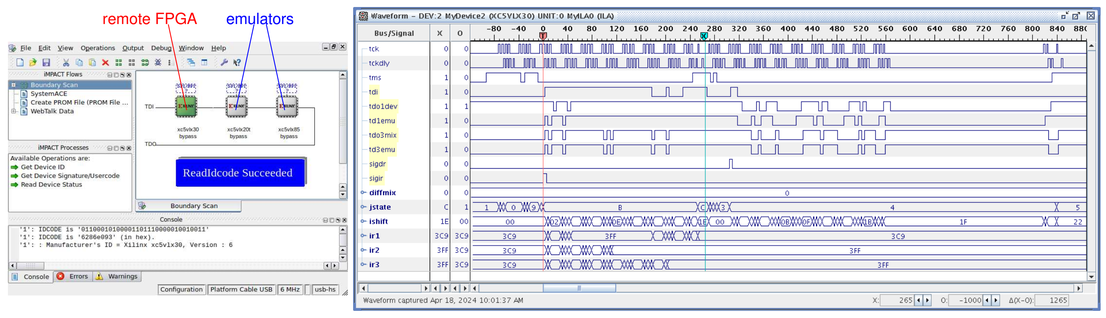


FPGA emulator logic

- FPGA emulator to handle minimal JTAG cycles: initialize chain, IR/DR (instruction/data register) cycles, read ID code, bypass mode
- FPGA emulator delays TDI to TDO by 1 TCK for bypass, 10 TCKs for IR cycles (for Virtex 5), 32 TCKs for DR cycles other than bypass

Result

- Two FPGA emulators inserted in the JTAG chain gained **230 ns** extra latency, measured in our test setup including some other overheads, when Xilinx Impact was operated at default 6 MHz.



6. Applications at Belle II

CDC FEE upgrade plan

- fully optical input (clock, trigger, and JTAG)
- Larger FPGA, i.e., faster JTAG programming solution is needed
- Second prototype to be produced soon, target replacement in 2026 or later
- Optical JTAG receiver is included in the design

FTSW upgrade plan

- New FTSW with optical clock, trigger, and JTAG distribution
- 14 QSFP ports, up to 48 optical connections to FEEs
- Optical JTAG receiver is included in the design
- Up to 48 optical JTAG drivers per module can be implemented
- First prototype just produced, target replacement in 2026 or later

7. Summary

- **New optical JTAG design was successfully demonstrated with a small test board**
- **New technique to overcome the JTAG latency was successfully demonstrated**
- **These solutions to be used in the planned upgrade of the Belle II readout system**

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