Hybrid Scrubber of SEM and Picoblaze for FPGA on COMET Read-out Electronics

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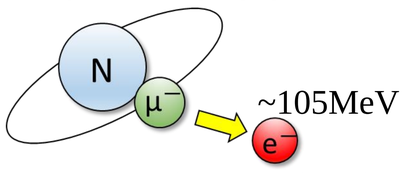
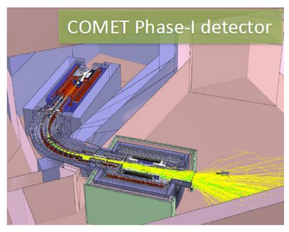
Introduction

J-PARC COMET Experiment



$\mu^- + (A, Z) \rightarrow e^- + (A, Z)$



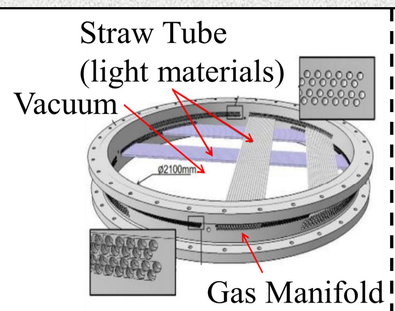
Purpose: Search for muon-to-electron conversion

- Undetectable physics process in the Standard Model [1]
- Single Event Sensitivity: $O(10^{-15})$ (Phase-I) $O(10^{-17})$ (Phase-II)

Straw Tube Tracker

To suppress the background and to achieve the goal sensitivity, we adopt this detector.

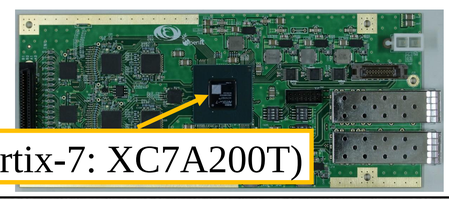
- momentum resolution: better than 200 keV/c



ROESTI(Read-Out Electronics for Straw Tube Instrument)

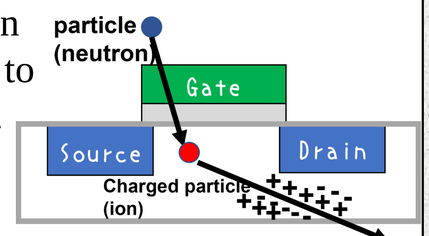
The ROESTI reads out the signal from the straw tube tracker precisely [2].

- installation location: in the gas manifold



Neutron Effect

- Neutron fluence (Phase-I): 1.0×10^{12} [n/cm^2](1 MeVeq) (Measurement time: 150 days)
- SEU (Single Event Upsets): Bit upsets in the FPGA configuration memory occur due to neutron irradiation.



Motivation

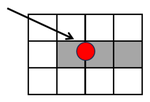
- Our conventional FPGA has adopted the 'SEM only' design for SEU mitigation.
- However, even with this design implemented, two types of UnRecoverable Errors (URE) occur as shown in the right.
- The purpose of this study is to develop a new SEU mitigation technique that resolves URE1 'Multi-Bit Upsets' and decreases the dead time.

URE (UnRecoverable Error)

SEUs have a potential to cause UnRecoverable Error (URE). URE cannot be repaired without re-downloading the FPGA firmware, which takes 37 seconds of dead time.

URE1. 'Multi-Bit Upsets'

The 'SEM only' design cannot correct multi-bit upsets (w/o adjacent double-bit upsets) in a configuration frame.



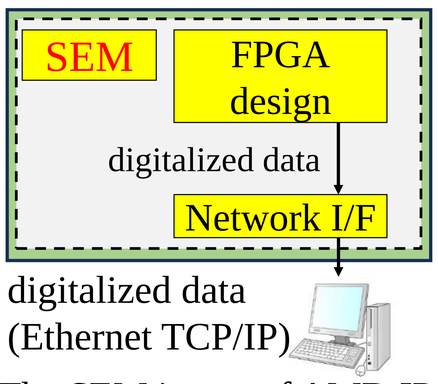
URE2. 'Other Errors'

An upset of a critical register can cause URE.
e.g. 1. registers in a clock generation module
2. registers in the SEM

SEU Mitigation Technique

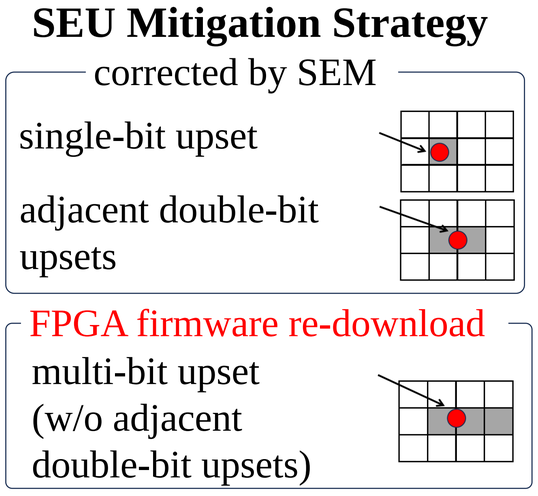
'SEM only' design

Block Diagram



*The SEM is one of AMD IP cores and used for detecting/correcting SEU errors [3].

SEU Mitigation Strategy



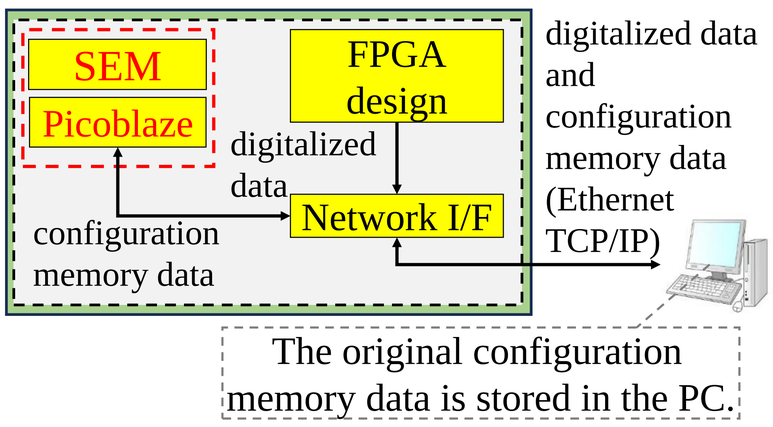
SEU Mitigation Technique

'Hybrid Scrubber' design

UPDATE

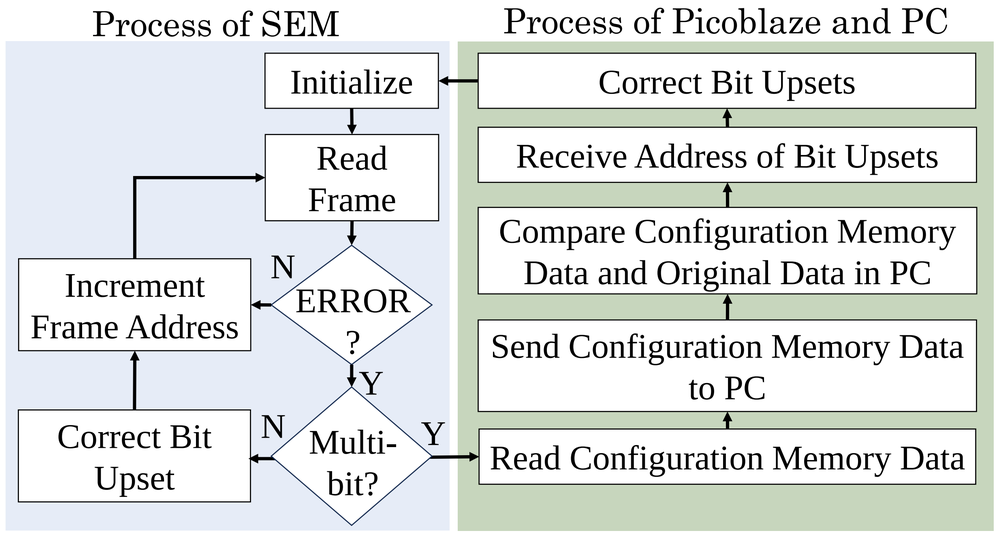
Hybrid scrubber of the SEM and the Picoblaze can correct not only single-bit upset but also multi-bit upsets!

Block Diagram

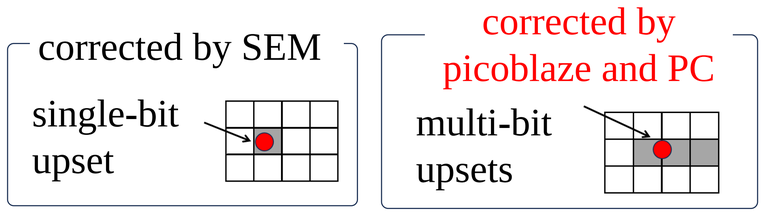


*The Picoblaze is the AMD soft microprocessor that enables reading/writing configuration memory bits [4].

Flowchart



SEU Mitigation Strategy



Features

- The size of the SEM and the Picoblaze is less than 1% of the total FPGA resources of the ROESTI.
- This design does not need a reference memory on the board.
- Updating from the 'SEM only' design to the 'Hybrid Scrubber' design does not add any components.

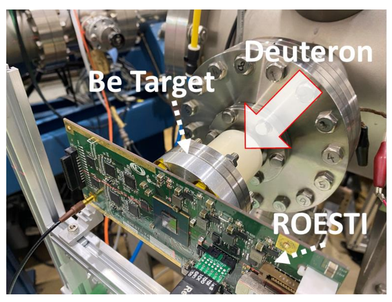
Neutron Irradiation Tests

Setup

By irradiating neutron beams, we tested the 'SEM only' design and the 'Hybrid Scrubber' design.

Facility:
TANDEM@Kobe Univ. (Japan)

- Beam: 3MeV Deuteron
- Target: Be (φ 20mm)
- Neutron energy: 2MeV (max. 7MeV)



Results

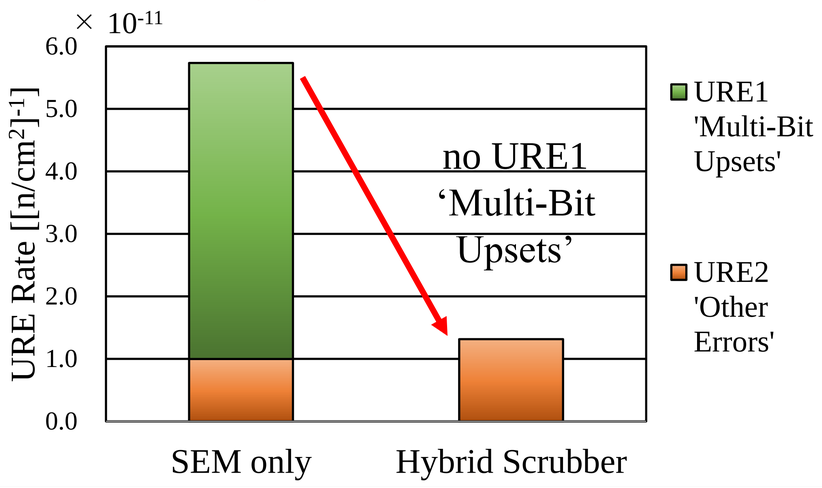
The URE rate decreased by 80%!

'SEM only' design

Total Neutron Fluence $[n/cm^2]$	4.01×10^{11}
#SEUs	1.01×10^{4}
#URE1 'Multi-Bit Upsets'	19
#URE2 'Other Errors'	4

'Hybrid Scrubber' design

Total Neutron Fluence $[n/cm^2]$	5.33×10^{11}
#SEUs	1.33×10^{4}
#repaired multi-bit upsets (w/o adjacent double-bit upsets)	20
#URE2 'Other Errors'	7



Conclusion

The 'Hybrid Scrubber' design can correct not only single-bit upsets but also multi-bit upsets.
The 'Hybrid Scrubber' design can decrease the URE rate by 80% compared to the 'SEM only' design. Because the frequency of FPGA firmware re-downloads can be reduced, the dead time decreases by 80%, and the Mean Time Before Failure (MTBF) is five times longer.

References: [1] Y. Kuno and Y. Okada, Rev. Mod. Phys. 73, 151-202, Jan.(2001)
[2] K.Ueno, et al., Nucl. Instrum. Meth. A , 936, 298-299, (2019)
[3] AMD Inc., "Soft Error Mitigation Controller" (PG036)
[4] AMD Inc., "PicoBlaze 8-bit Embedded Microcontroller User Guide" (UG129)

Acknowledgement: This work was supported by World Premier International Research Center Initiative (WPI), MEXT, Japan.
The authors would like to express their sincere thanks to the staffs of The Tandem Accelerator Laboratory of Kobe University.