The Front-End Electronics for the Hyper-Kamiokande Far Detector

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***Abstract*—A new front-end board has been designed and developed for the photomultipliers used in the Hyper-Kamiokande experiment, the new generation water Cherenkov detector in Japan. The Hyper-Kamiokande far detector will be instrumented by 20000 Hamamatsu R12860 PMTs, a new and improved version of the photosensors used in the previous experiment Super-Kamiokande. These PMTs have been specially developed by Hamamatsu to create a sensor that improves the quantum efficiency and the ability to withstand higher pressures that will be present in Hyper-Kamiokande. The new PMT electronics will be placed in a pressure vessel alongside the PMTs underwater. The use of new photosensors and the use of underwater vessels require the development of a new board with improved digitizing capabilities and a long life expectancy.**

This work describes the design and features of the new digitizer front-end board designed for Hyper-Kamiokande. From the stringent requirements imposed by the collaboration, to how the board was designed, and concluding with the tests performed on the last proven prototypes before mass production.

***Index Terms*—Analog circuits, Neutrinos, Photomultipliers, Readout electronics.**

I. Introduction

THE Hyper-Kamiokande (HK) experiment is at the forefront of next-generation research on neutrino oscillations, nucleon decay, and astrophysical neutrinos. This avant-garde detector, nestled deep underground in Japan, is the third in a lineage of water Cherenkov detectors. It will serve as the far detector for a long baseline neutrino oscillation experiment planned for the upgraded J-PARC neutrino beam as well as a detector capable of observing proton decays, atmospheric neutrinos, and neutrinos from astronomical origins enabling measurements that far exceed the current world best measurements made by Super-Kamiokande (SK) [1].

Hyper-Kamiokande consists of a cylindrical tank, with a water depth of 71 m and a diameter of 68 m. One of the key detector parameters that determines the event statistics in neutrino observation is the detector mass [2]. HK will have 259 ktons of water as a medium to detect neutrinos, of which 188 ktons is fiducial volume, 8 times more than SK. The particles, interacting with water, will generate Cherenkov light that will be captured by the 20000 Hamamatsu R12860 PMTs placed on the detector walls. These photomultipliers will grant 20% of the photo-catode coverage.

The new R12860 photomultipliers (Fig. 1a) have been developed by Hamamatsu, for HK, to improve the one used by SK [4]. The two main differences between the two models are the change of the dynode structure to a box-and-line one and the higher quantum efficiency, with a peak of 30%. Also the resistance to pressure has been improved, with the new PMTs able to withstand to a pressure of 1.25 MPa waterproof.

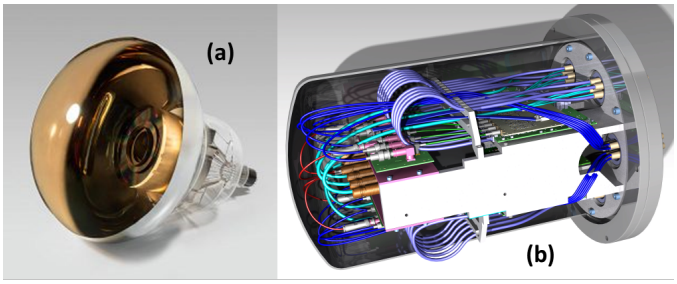
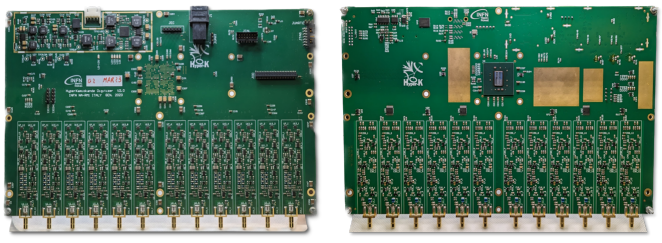


Fig. 1. New 20" Hamamatsu R12860 PMT (a) developed for Hyper-Kamiokande and the underwater vessels that will contain the electronics (b).

Unlike Super-Kamiokande, in HK the readout electronics will be placed in underwater vessels next to the PMTs (Fig. 1b), occupying the empty spaces between them along the cylinder walls. This choice has been made to reduce the cable length that will connect the PMTs to the front-end (FE) boards, to minimize signal degradation.

Due to the new photomultipliers and the new arrangement inside the vessels, a new FE digitizer board was required. The one used in SK was based on obsolete components that did not take full advantage of the improved technology of the R12860 PMTs. In particular, the SK digitizer could not meet the requirements for sampling rates, charge and timing resolution. In addition, it dissipates more than 1 W per channel, resulting in overheating the water in the tank. The shape of the SK board is also a problem, as it is too large to fit into the small underwater vessels designed, so at least the whole board had to be redesigned. The latest prototype produced to overcome all these issues is shown in Fig. 2.



(a) *(b)*

Fig. 2. The latest digitizer prototype front (a) and back (b).

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II. Board Requirements

Hyper-Kamiokande aims to detect a broad spectrum of events, having energies from a few MeV to several hundred GeV [2]. This results in interactions that generate events of single or few photo-electrons (p.e.) to more than 1000 p.e. So one of the fundamental requirements is a wide charge dynamic range, from 0.1 p.e. to 1250 p.e., with a charge resolution of 0.05 p.e. for signal smaller than 10 p.e., and better than 0.5% for signals bigger than 10 p.e.

To precisely detect the Time-of-Arrival (ToA) of the photons generated by the neutrinos interacting in water, a time resolution of at least 0.3 ns for signal under 5 p.e. is required. The time resolution is defined as the FWHM of the time measurement and is intended for both coincident and absolute time measurements.

Some type of events can generate triggers on the same PMT multiple times and in rapid succession. This is the case of supernova explosions, the closest of which can produce up to 90000 events in a burst of a few tens of seconds. In these cases the frequencies can reach $10^6 - 10^7$ Hz [5]. Therefore, a dead time of at least less than 1 μs is essential for capturing these types of events.

The final requirement, dictated by the placement of the electronics in sealed containers, is low power consumption and a low failure rate for all electronic components. Hyper-Kamiokande will be operational in 2027 and is expected to continue taking data for 20 years without maintenance, so components with a lifetime of at least 20 years of continuous use must be used. Excessive heat dissipation in the water (more than 1 W per channel) can create convective currents and affect the detector's reconstruction capabilities. For these reasons, a maximum power consumption of less than 1 W per channel and an expected failure rate of 1% in 10 years have been specified.

All these requirements are summarized in Table I.

TABLE I
Hyper-Kamiokande Front-end Board Requirements

Timing resolution	less than 0.3 ns @ 1 p.e. less than 0.2 ns @ 5 p.e.
Charge resolution	0.05 p.e. under 10 p.e. better than 0.5% above 10 p.e.
Charge dynamic range	0.1 to 1250 p.e.
Power dissipation	less than 1 W each channel
Reliability	20 years of lifetime and 1% failures in 10 years

III. The Board Design

Among the different designs proposed by the collaboration for the photomultipliers FE boards, a solution based on discrete components was chosen. This was judged to be a suitable choice for this application, as opposed to other solutions such as the one adapted from Super-Kamiokande or newly developed ASICs, due mainly to costs and technology used. The total number of digitizer boards in HK will be around 800, so producing an ASIC for such a small number of boards does not take advantage of the economies of scale inherent in integrated circuits, not to mention the time needed to update and improve such a design, too risky for a construction schedule such as the one imposed by the Hyper-Kamiokande collaboration [3]. The technology used in ASICs is also less versatile, in the discrete design proposed CMOS, BJT and FET-based components are used, which are impossible to achieve together with an ASIC design.

The current design is triggerless and has 12 single channels that digitize the analog signal from the photosensors and send them to a Xilinx Kintex-7, an FPGA that reconstructs the measured signals and transmits them to a concentrator board called the Digital Processing Board (DPB) using a Mini SAS cable at a maximum rate of 3 Gbit/s. The DPB then will send data outside to the data acquisition using optical fibers. The FPGA also manages the board slow control, calibration signals and restores the integrator baseline, as will be described in the next sections.

The board is powered at 12 V by a power supply board present in the vessel. All the voltage rails needed by the components and the FPGA are derived on board using a switching converter circuit.

The single channel digitization path can be divided in 3 blocks: the input receiver and protection circuit, the timing path and the charge path. The schematic and connections of these blocks is illustrated in Fig. 3.

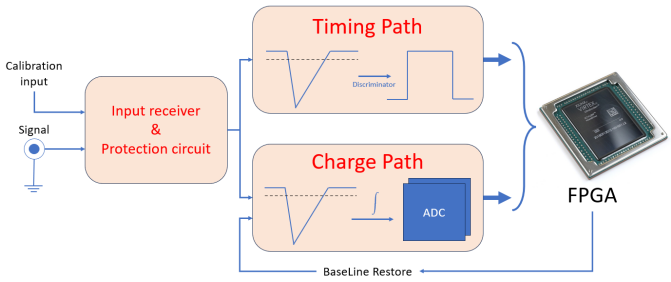

Fig. 3. Block scheme of the front-end single channel board. The signal goes through the input receiver, then splits to the timing and the charge path, the outputs are then read by the FPGA.

A. Input Receiver and Protection Circuit

The initial component of the individual channel front-end is the input receiver. Typically, an input stage in an FE system consists of a buffer and a filter to optimize the signal-to-noise ratio and ensure compatibility with the 50 Ω cable impedance. In the case of a PMT, a protection circuit is additionally required to prevent the signal from exceeding the the absolute maximum input voltage of the FE's integrated circuits. Also a calibration input is present, it will be described in a later section. This signal can be enabled using a logic signal by the FPGA. The whole schematic is in Fig. 4.

The circuit design for the input receiver is based on the PMT sample waveform. Key waveform characteristics considered are the rise time and signal width. All R12860 PMTs are gain equalised with a voltage measured for each photo-detector to

give a gain of 10^7. This value was chosen as a compromise between good amplification of small signals (few p.e.) and better performance of the PMTs. With this bias voltage, the worst-case signal was considered when designing the input stage, i.e. a signal generated by 1250 p.e., the rise time was found to be less than 10 ns, and the signal width was less than 50 ns. To buffer this fast signal at the input, a high-speed buffer is required, typically consuming significant power. To minimize the high frequency noise a Low Pass Filter (LPF) RC has been placed as the first stage in the chain, with a chosen frequency of 20 MHz. This filter also allowed the use of lower power, slower operational amplifiers, further reducing the power consumption of each channel. The LPF ensures impedance matching with the cable across the entire frequency range, not just in the high-frequency range. To better achieve this, an input crossover filter has been designed operating at 20 MHz. The low pass filter matches the impedance at low frequencies, while a High Pass Filter (HPF) matches the impedance at the high frequencies. To adapt the filters to the input cable a $100\,\Omega$ resistor is used in parallel with the $100\,\Omega$ filter impedance in a current divider configuration. This resistor can be easily swapped to adapt the precise cable impedance to the board. This adaptation will be made during construction using the impedance value of each batch of cable given by the manufacturer. Another advantage of having a filter preceding the buffer is the reduction of the amplitude of the signals, to a maximum value of $\sim 4.5\,V$, thus allowing the circuit to be powered with a 10 V supply instead of 12 V without saturating the operational amplifiers used. In order to match the cable signal, the length and width of the PCB traces have also been optimised to provide the correct impedance.

To ensure protection against sparks and large signals, a protection circuit is necessary for the FE circuit. The primary components used for protection are clamping diodes, which limit the voltage on subsequent components to a fixed value. In our design, the limit was set at 10 V. However, clamping diodes alone cannot safeguard against high current pulses resulting from HV discharges. To address this issue, a current limiter resistor is utilized before the diodes. This resistor must be able to withstand high voltages, and a TVS (Transient Voltage Suppressor) diode has been added to better protect against these spikes. The TVS is added after the filter, with its parasitic capacitance in parallel with that of the crossover filter, in order to reduce the problems it could cause in the final signal adaptation. A gas discharge tube is also used to protect the components close to the connector; this component was chosen instead of another TVS because of its low parasitic capacitance, although its performance is inferior to that of a TVS. The scheme of the input buffer and the protection circuit is shown in Fig. 4.

B. Fast Discriminator Path

The fast discriminator is necessary to generate a logic signal that will be sent to the FPGA to start the acquisition and to generate the time stamp using a TDC. The fast discriminator is internally composed by three components: the fast amplifier, the Baseline Restorer (BLR) and the discriminator.

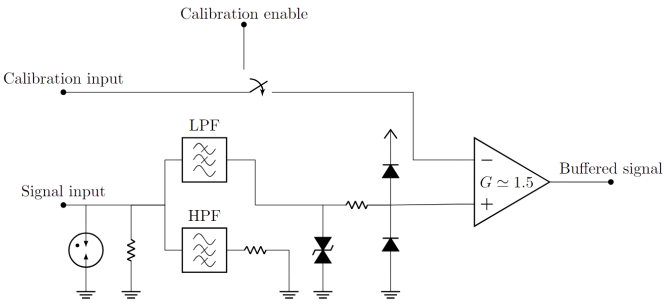

Fig. 4. Signal and calibration path block diagram. On the top is the calibration path, enabled by a signal generated by the FPGA. On the bottom is the signal input path, composed of various components that adapt and filter it.

The fast amplifier is a high gain amplifier, with G $\simeq$ 40. Two configurations were initially developed, one based on three operational amplifiers and one based on a BJT transistor and an operational amplifier. It was observed that the first design tends to oscillate when in saturation, and this could generate a trigger during the acquisition window of the previous event. To overcome this problem, a solution that uses a BJT has been considered. This also uses an operational amplifier to improve the oscillation and the time it takes to return to the initial state after amplifying a signal that has saturated it. A scheme of this amplifier is in Fig. 5. It consists of a BJT and an operational amplifier connected to the collector of the transistor. The output is connected to the emitter of the BJT to form a feedback loop. This configuration provides a higher input impedance compared to an equivalent, simpler op-amp based inverting circuit.

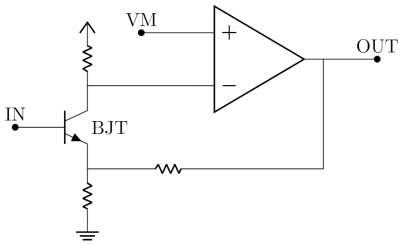

Fig. 5. The BJT based amplifier with $G \simeq 40$ used in the fast discriminator path. VM is a constant voltage.

The next section of the circuit is the BLR. This component is essential since the signal is AC coupled from the receiver, consequently the baseline could depend on the signal rate. We developed a classic BLR consisting of four diodes and two current generators, realised with two resistors, to simplify the design instead of using more complicated circuits such as a current mirror. An offset voltage of about 1 V has been introduced to avoid using negative voltages for the discriminator. The signal after the BLR is fed into the discriminator that generates the logic signal for the FPGA; the threshold is programmable through a DAC controlled by SPI. The PCB path length from the discriminator to the FPGA is critical, so needs to be equalized for all the 12 channels during the initial PCB design. The whole fast amplifier schematic is shown in Fig. 6.

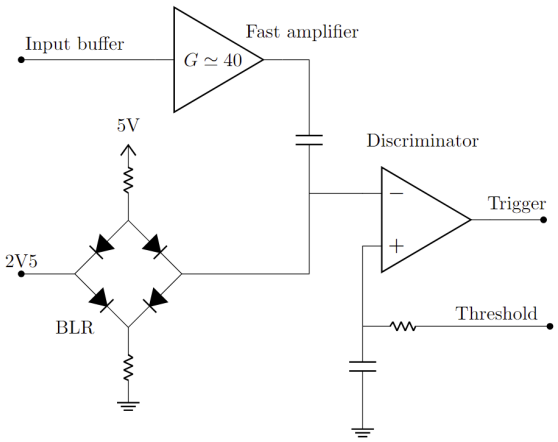

Fig. 6. Fast amplifier whole simplified schematic. The signal coming from the input buffer is greatly amplified and then added to the BLR and fed to the Discriminator. Based on the Threshold set using a DAC, a digital Trigger is generated and sent to the FPGA.

To reduce dead time, a new technique called Multi-Time-over-Threshold (Multi-ToT) has been implemented in the FPGA firmware. The main source of dead time in the FE is the charge measurement. The signal has to be shaped, integrated and measured by ADCs and this process takes time. Instead, the timing path needs only the time it takes the signal to pass through the components to create the logic signal. To take advantage of this, the FPGA still receives triggers from the timing path during charge conversion, triggers from events that would otherwise not have been detected, but only measures its ToA and ToT. Later, during offline analysis, it is possible to reconstruct the charge measurement from the ToT if the board has been correctly calibrated. The Multi-ToT has also been tested and implemented on HK's other FE boards and has shown to significantly reduce dead time.

C. Integrator Path

The integrator is the fundamental block in the acquisition chain, since the charge resolution depends on it. The design of this block proved to be a real challenge due to the very stringent specifications it had to meet. The main challenges of an integrator scheme based on an operational amplifier are the reset mechanism and the fixing of the operating point to avoid the integration of unwanted currents. The ideal circuit is always in integration and this is not possible with pulse signals like the ones from PMTs. Also, a very stable baseline is needed to keep homogeneity in the acquired values also at different signal rates.

The easiest way to stabilize the baseline value is to include a feedback system in the circuit, this will constraint the voltage value on the input of the circuit at a predetermined value, which in this case was set at 200 mV. The problem with this solution is that the system would also keep the voltage to the fixed value during the acquisition of a PMT signal. The solution is to open the feedback just before the integration of a signal, this is done using a logic signal called BLR_Enable. This signal is generated by the FPGA and the time needed for it to be read and managed is ∼15 ns; for this reason a passive delay line (DL) of 25 ns that connects the input buffer to the integrator is present. Before the DL, the signal is filtered with a LPF at 10 MHz. The filter also reduces the signal amplitude, so to balance this effect the signal is amplified once again before being fed to the integrator.

There are 4 phases to an acquisition, as shown in Fig. 7. When the logic signal generated in the fast amplifier block triggers the FPGA, it generates the signals for the integrator and the ADC, in time not to lose the signal due to the closed feedback (phase 1). The BLR_Enable signal is by definition asynchronous and is generated immediately after the fast path trigger, so it is generated in the FPGA using combinatorial logic. The FPGA then generates the hold signal for the ADC to start acquisition (phase 2). After a programmable delay, the FPGA logic also starts the integrator reset, completing the reaction. As the ADCs used are sample-and-hold, they store the peak value internally during acquisition, so there is no need to wait for the full signal to pass after the peak before resetting the integrator (phase 3). During this conversion, the integrator path is blocked, while the fast path can still receive triggers to take advantage of the multi-ToT technique. Finally, after the ADC has completed the conversion, the channel is ready for the next event (phase 4).

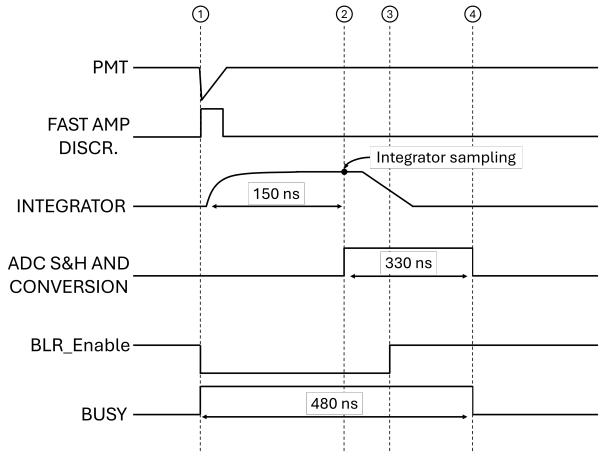

Fig. 7. Digitizer board circuit timing diagram (not to scale) with the 4 phases showed.

The frequency response of the whole integration circuit has also been studied. The system was designed with a very tight bandwidth, with a low cutoff of 1 MHz and a high cutoff of 4 MHz. This helps in minimizing the low frequency shift and also the high frequency noise that can enter in the circuit. A simplified schematic of the integrator previously described is in Fig. 8.

The integrator signal is acquired by two independent Analog-to-Digital converters, the MAX11108, 12-bit ADCs capable of converting at a maximum rate of 3 Msps. One ADC is preceded by a unitary gain buffer and one by an amplifier with a gain of 8. This choice was a consequence of the huge dynamic range of the PMTs, to be acquired with a very high resolution. For small signals, such as those produced by a few p.e. of ∼20 mV, the resolution must be even better, since photon counting is still possible. The buffer at G = 8

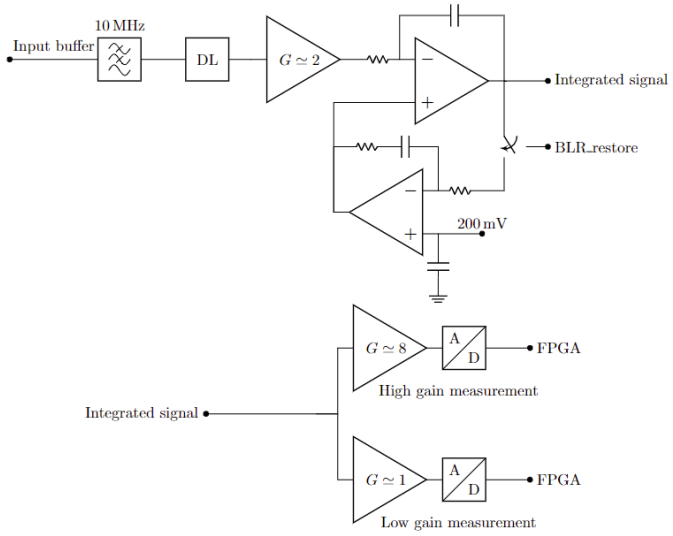

Fig. 8. Integrator schematic. The signal from the input buffer goes through the LPF the DL and the 2-gain amplifier before being integrated and fed into the ADCs. The integrator is connected to the feedback loop that restores the measured baseline via a switch, controlled by the FPGA and opened just before the signal arrives.

acquires the small signals with the highest resolution, while the other buffer covers the entire dynamic range with a lower resolution. It is important to say that, for each event, both gains are acquired and stored, only in software is it possible to choose the most suitable value between the two.

D. Calibration Circuit

A calibration circuit is present on the digitizer board, as requested by the collaboration. The circuit is able to create different signals, similar to PMTs, using a switch that creates a pulse switching from ground to a DAC output voltage called V_{DAC}, controlled by the FPGA. The DAC used is the DAC70501 from Texas Instrument, a 14 bit Digital-to-Analog converter configured to generate signals up to 3.6 V. Before being distributed to the channels, the signal goes through a buffer and then through a multiplexer. The latter, also controlled by the FPGA, selects between 4 signals: the buffer output directly, and the buffer output attenuated 3, 9 and 18 times. This technique allows small signals, such as that generated by 1 p.e., to be created without letting the switch generate them using a very small signal from the DAC.

The pulse then is filtered again and amplified 3.5 times to generate signals that cover all the charge dynamics. Then it is fed to 4 buffers that distribute it to the channels. The path from the last buffers to the amplifier in the input receiver also is a critical path in the board design and all the 12 paths are equalized.

The schematic of the calibration circuit is shown in Fig. 9

IV. Board Performance

Ten boards of the latest prototypes have been built (Fig. 2) and are currently under test. To verify that they comply with the requirements in Table I several tests have been performed.

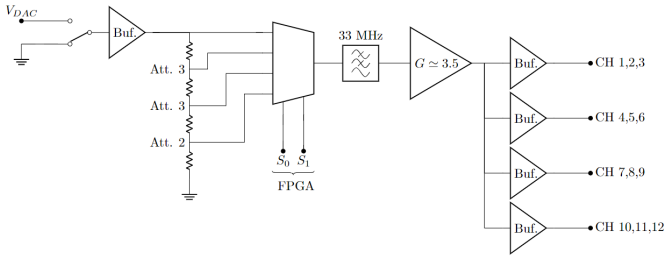

Fig. 9. Calibrator block diagram.

The timing resolution is measured to be complying with the requirement both in case of 1 p.e. and 5 p.e. signals. The resolution is ~ 0.2 ns for smaller signals and gets only better for signals with bigger charge, as shown in Fig 10.

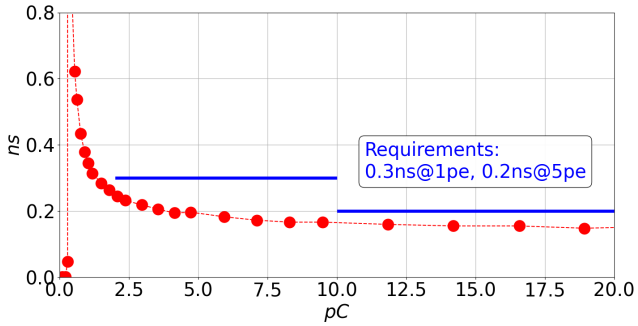

Fig. 10. Timing resolution for signals having different charge. The single p.e. is at ~ 1.8 pC.

To test the charge resolution, signals having different total charge have been measured, at an integration time of 200 ns, i.e. the time set for the signal integration. The charge measurement circuit is able to measure charge with a resolution of ~ 0.15 pC (Fig. 11)

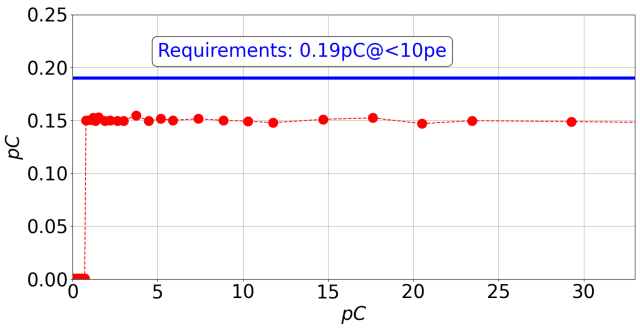

Fig. 11. Charge resolution for signals of different charge at 200 ns of integration time. The single p.e. resolution is at 0.15 pC.

During the normal workflow, the inside of the vessel will heat up, due to the number of electronic components dissipating heat. The vessel is passively cooled using a plate acting as a heat sink in contact with the temperature controlled water of the HK tank, that is kept at 15°C. Measurements made in water showed that the maximum temperature reached in the vessel

is 25°C. To test the board behavior at higher temperature, the charge linearity was measured at different temperatures, from 25°C to a maximum of 38.5°C, which is the temperature chosen as the maximum attainable working point inside the vessel. The results show that the linearity does not change at every temperature tested, as in Fig. 12.

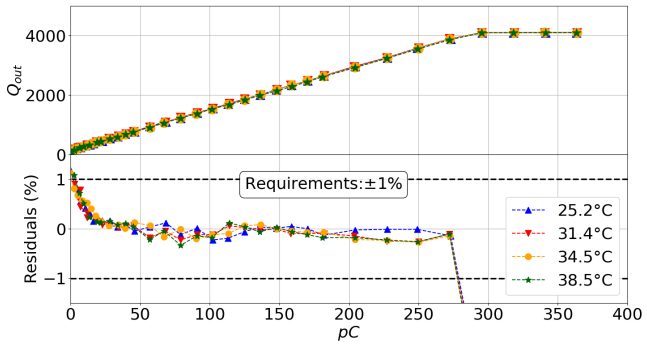

Fig. 12. Charge measurement temperature dependency, at different temperatures, from 25°C to 38.5°C. On the bottom the normalized residuals from the linear fit made for each temperature. The requirement is within ±1%.

The latest prototypes showed a power consumption of ≃ 220 W per single channel, well below the requested 1 W. This astonishing result has been achieved through the selection of low power components and a commitment to using as few components as possible.

In terms of average board life and failure rate, an MTBF calculation was made at the initial design stage using dedicated software and the Siemens SN 29500 standard. The result is an MTBF of 1.32×10^7 hours for an expected lifetime of 2×10^5 hours. This proved adequate and was approved with the design. However, in the years since the final design was developed, the components on the board have changed, so this calculation will be repeated using the same software before the detector assembly begins. In addition, a Highly Accelerated Lifetime Test will be carried out on some test digitizer boards throughout the assembly process over the next months, monitoring them at ≃ 70°C.

V. Conclusions

Hyper-Kamiokande will start data taking in 2027. Due to the new photomultipliers used and to the positioning of the front-end electronics in the water tank new readout electronics and a new front-end were needed. The new electronics must have a large charge dynamic range, measured with a resolution of 0.05 p.e., and also a 0.3 ns resolution for timing measurements. The power consumption must be minimal to avoid any convection currents in the tank water and to increase the average life of electronic components. The latest prototype produced in March 2023, and currently under test for the most recent design controls, complies with all the requirements imposed by the physics of the experiment. In the coming period, the final tests will be carried out on the average life of components to ensure their operation for 20 years. The final design should be finalized by the end of 2024, and the mass production will commence by the end of 2024 and beginning of 2025.

Acknowledgment

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