The front-end electronics of the Hyper-Kamiokande Far Detector
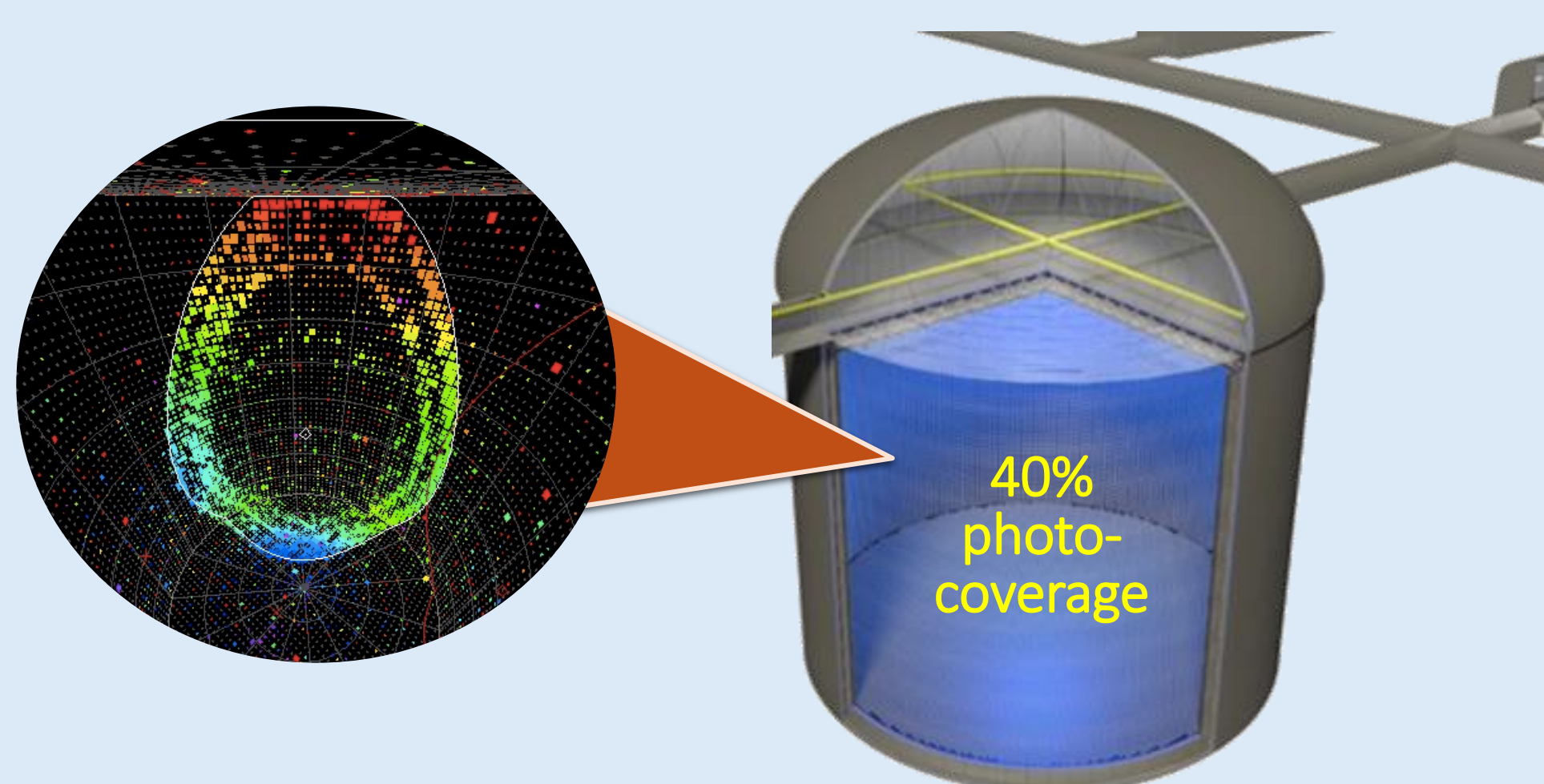
Alessandro Di Nola on behalf of the Hyper-Kamiokande Collaboration

Università degli studi di Napoli Federico II

Hyper-Kamiokande

Hyper-Kamiokande (HK) is the next generation Water-Cherenkov detector with multi-purpose scientific goals:

- Investigation on **CP-violation** in leptonic sector;
- Neutrino **oscillations** (atmospheric, accelerator and solar);
- Determination of the neutrino mass ordering;
- **Proton Decay**;
- Observation of astrophysical neutrinos.

40% photo-coverage

The readout electronics

Board requirements

- A timing resolution of less than 0.3ns@1pe (photo-electron) and less than 0.2ns@5pe
- A charge resolution of 0.05 pe under 10 pe and more than 0.5% above 10 pe
- A charge dynamic range from 0.1 to 1250 pe
- Low power dissipation (less than 1 W for each channel)
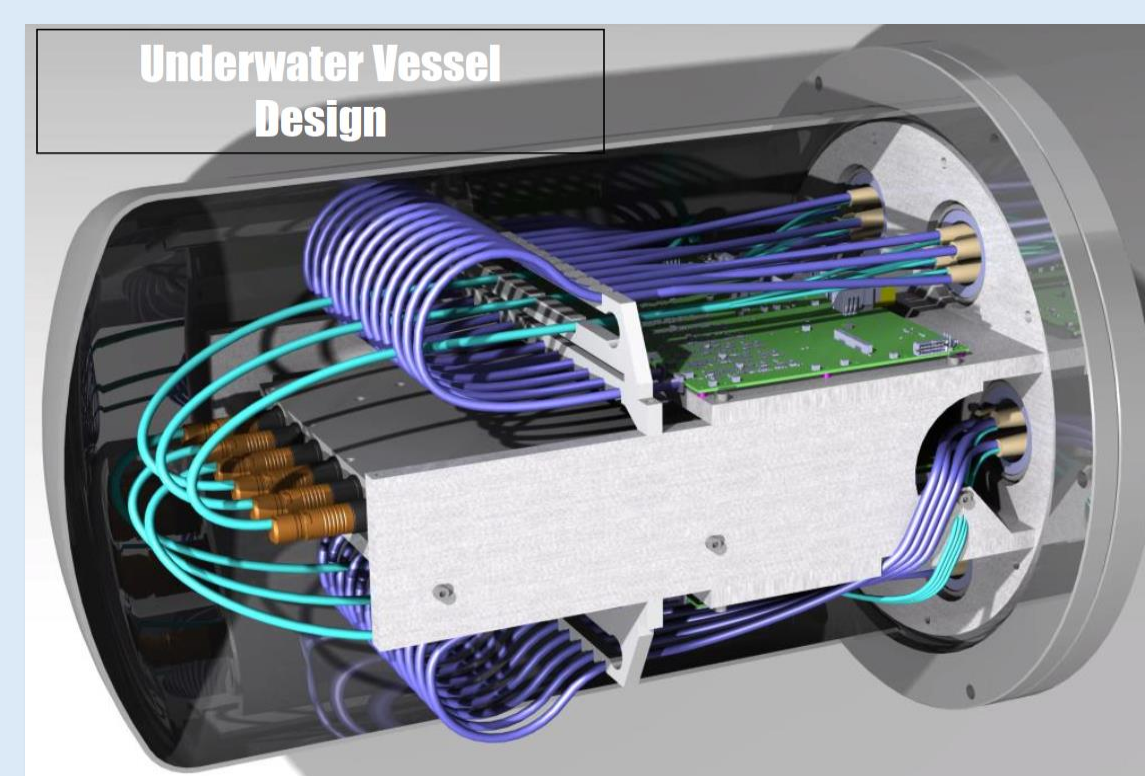- Low expected failures (about 1% in 10 years)

The detectors

Hyper-Kamiokande uses the new **R12860 PMT 20''** box-and-line PMT developed by Hamamatsu. These PMTs are based on the Super-Kamiokande PMT design and improves it significantly.

20" B&L PMT

Vessel design for the 20" PMTs electronics

Unlike Super-Kamiokande, in HK the electronics will be inside the tank, to be closer to the detectors. This required the design of an underwater pressurized **vessel,** that contains 2 digitizer boards, the concentrator board called Digital Processing Board (DPB), and the power supply boards (high and low voltage).

Single channel

The single channel is designed using discrete components and can be divided in three main blocks :

- **The input receiver**, used to protect the components from PMT discharges, to adapt the impedance of the PMT cable and to limit the bandwith of the input signal
- **The integrator circuit**, that converts charge into a voltage which is sampled by 2 12bit-ADCs, one for High Gain (HG) one for Low Gain (LG)
- **The timing measurement circuit,** that uses a discriminator to generate a digital signal that is used from the FPGA to measure Time-of-Arrival and Time-over-Threshold
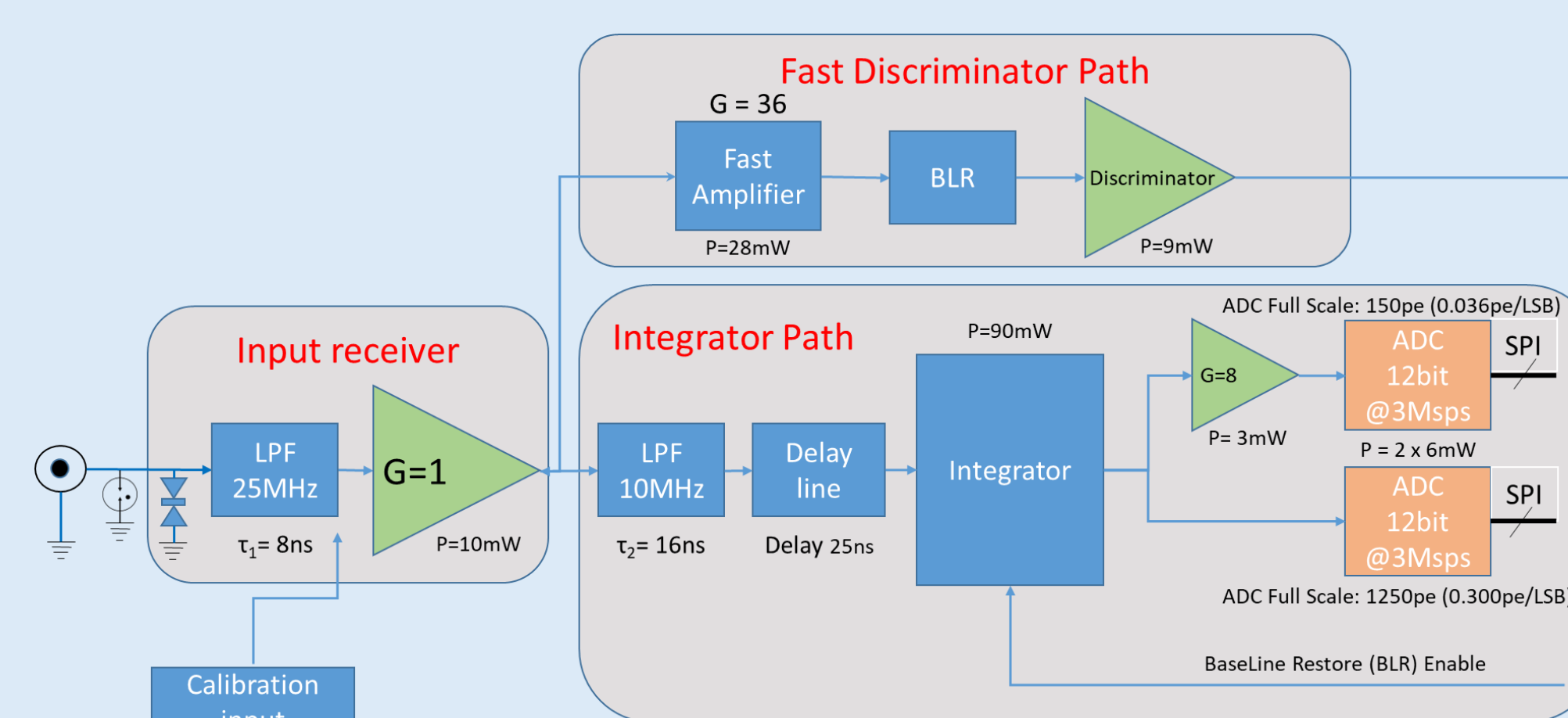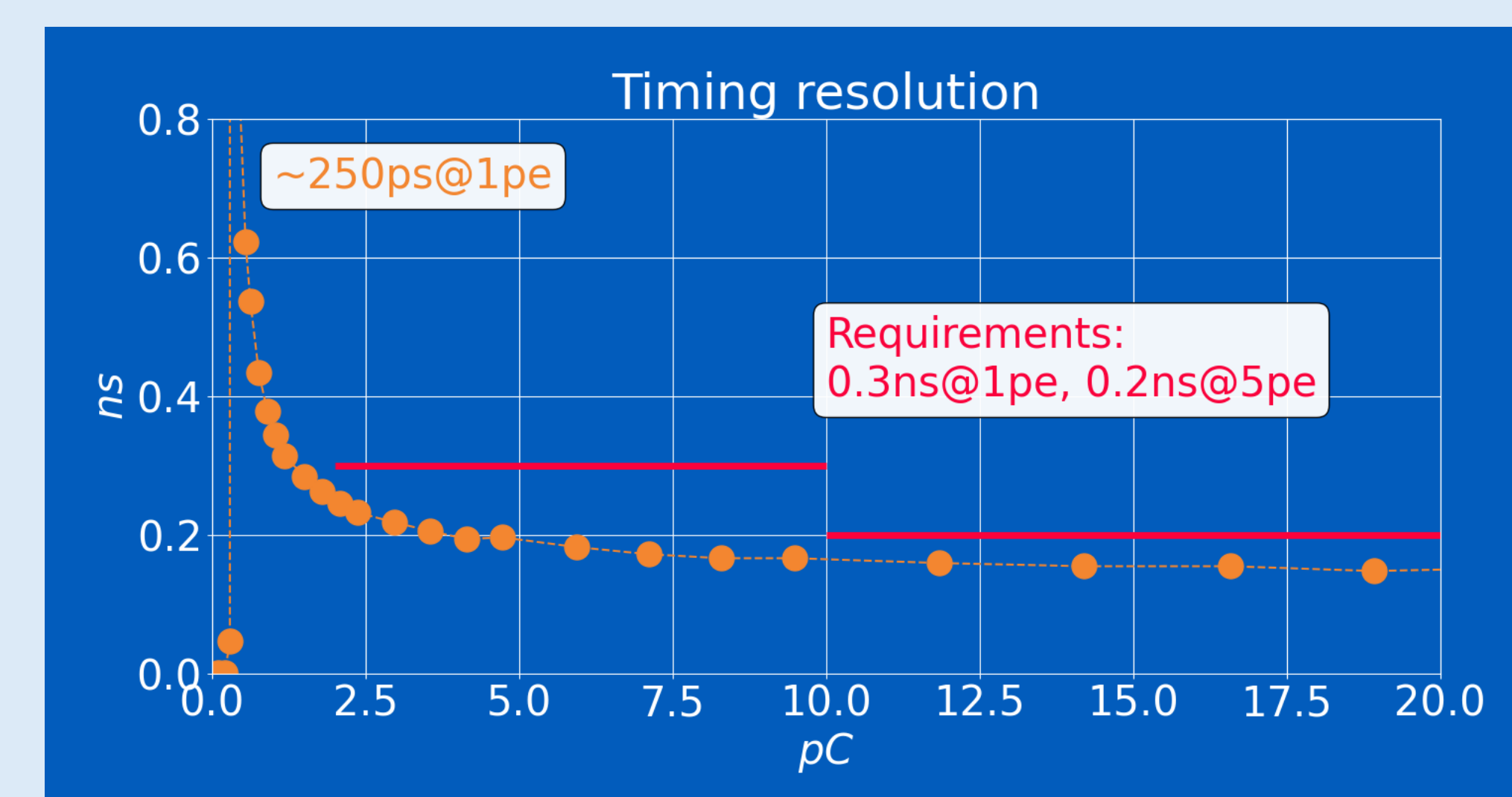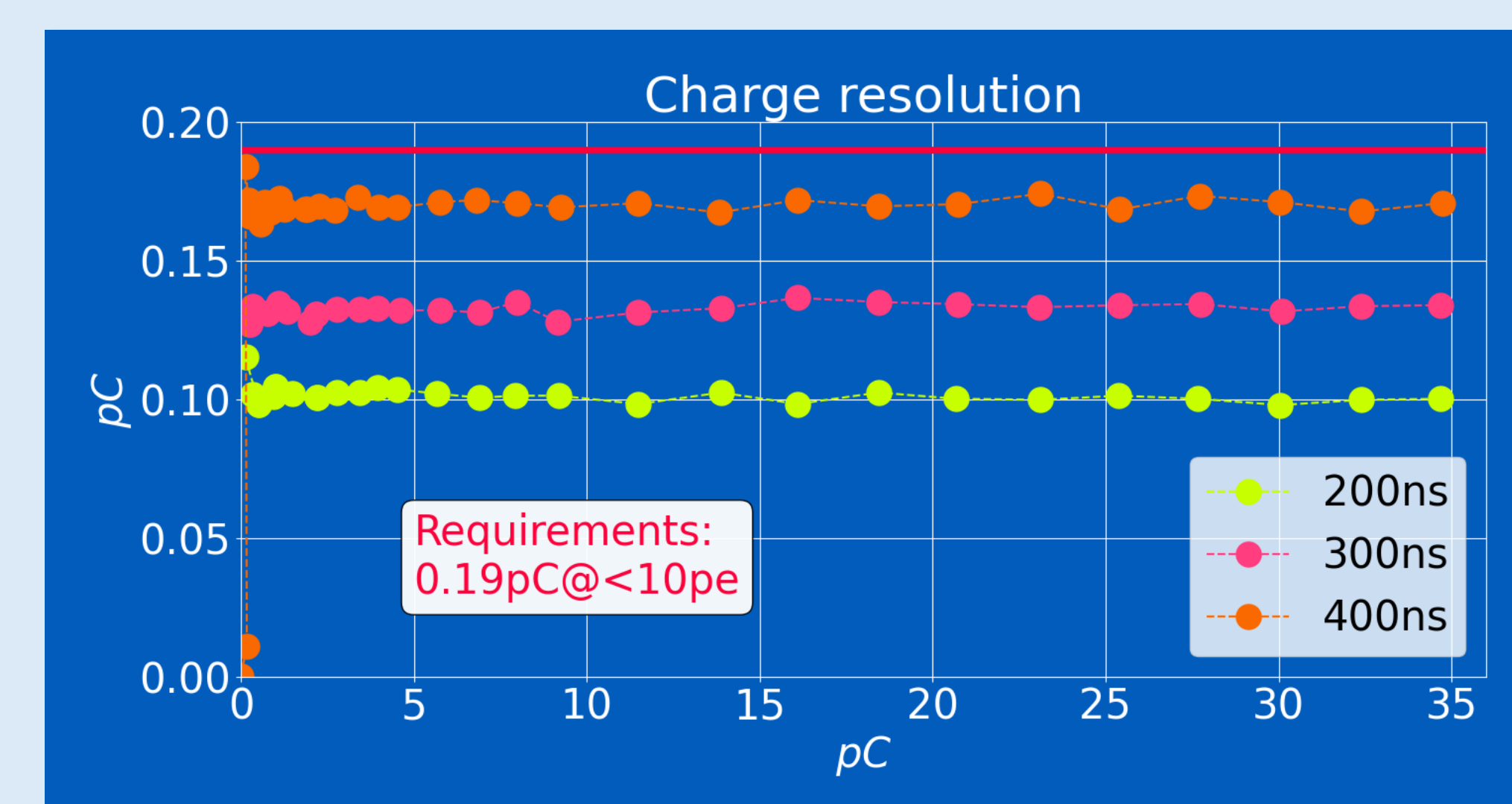
Performances

The system is stable for a wide range of temperatures. During the experiment the vessel will be in contact with temperature controlled water so we expect a temperature gradient in the vessel that reaches around 25°C.
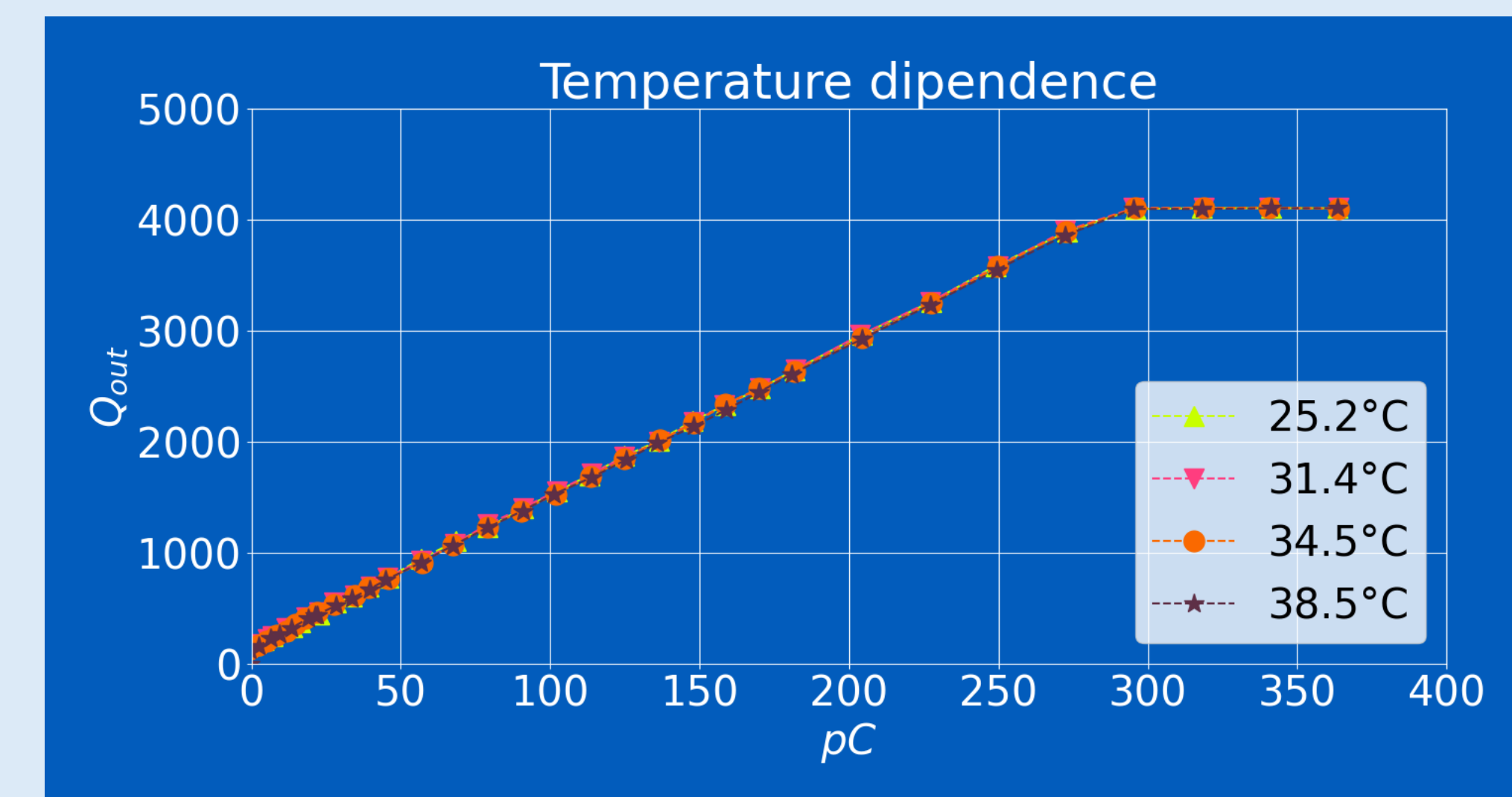
The timing measure made by the FPGA has a resolution of ~0.2ns for 1 p.e. and gets better at a large number of p.e., as expected by theory.
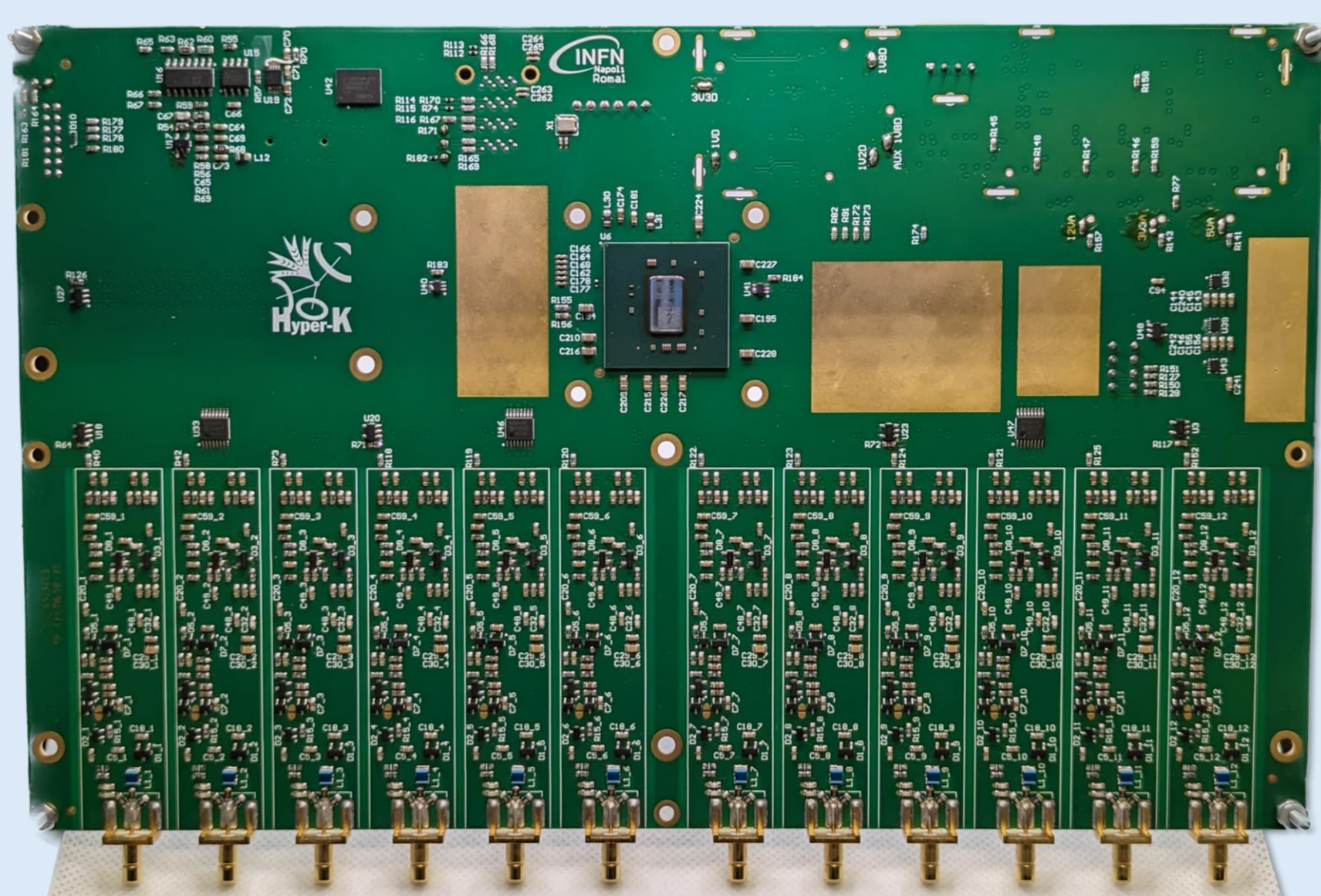
The charge measurement circuit is able to measure the charge with a resolution of ~0.1pC for a faster integration time of 200ns, and about 0.17pC at 400ns.

Conclusions

- The digitizer complies with the requirements. Prototypes are currently under test and they are working as expected.
- The design will be finalized soon and mass production will start shortly after.

My contacts

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