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A high-precision two-stage Time-to-Digital Converter in 180 nm CMOS Technology

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In the field of particle physics experiments, Time-of-Flight (ToF) is a powerful tool to perform particle identification, and the Time-to-Digital Converter (TDC) plays a crucial role in the high-precision time measurement. As the momentum of the particles to be studied increasingly goes high, the time resolution requirement becomes higher accordingly, and the TDC is expected to achieve picosecond (ps) time precision. Moreover, high-resolution measurements are also widely demanded in other scientific domains, such as LIDAR, TOF-PET, etc. In this work, the design and testing of a 16-channel coarse-fine hierarchical TDC is present. It utilizes a two-level conversion structure combined with a coarse counter to achieve a wide dynamic range with high time resolution. The coarse time is measured with a shared two-edge counting gray counter, and the fine time is obtained with a dedicated two-stage TDC, which is composed of a delay line TDC and a Vernier TDC. The bin size of TDC is approximate 7 ps. To implement a low-jitter clock generation circuit with a small area, a multiplying delay-locked loop was employed, and with a fixed pattern noise calibration, the clock jitter was achieved better than 3 ps. The ASIC was implemented in a standard cost-effective 180 nm CMOS process, and test results show that the TDC reaches a dynamic range of 5 μ s with 8.5 ps precision for all channels, while utilizing less than 10 mW/chn.

Minioral

Yes

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No

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No

Author: QIN, Jiajun (University of Science and Technology of China (CN))

Co-authors: Mr GUO, Donglei (University of Science and Technology of China); Mr LI, Jiaming (University of Science and Technology of China); Mr ZHAO, Junbo (University of Science and Technology of China); Dr ZHAO, Lei (University of Science and Technology of China (CN)); Mr LI, Zhuang (University of Science and Technology of China)

Presenter: QIN, Jiajun (University of Science and Technology of China (CN))

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