An FPGA-Based High Precision Pulse Width Measurement Time-to-Digital Converter with Time Division Multiplexing Encoder

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Introduction

- **FPGA-based TOT Measurement TDCs in High-Energy Physics:** TDCs are vital for high-energy physics experiments. FPGA-based TDCs offer advantages like increased channel density and reduced power consumption.
- **Challenges and Optimization:** Conventional TDL TDCs face limitations in capturing rising edges only. Optimization strategies involve resource-intensive methods, but they compromise resource usage, channel density, and measurement throughput.
- **Novel Architecture and Performance:** The dual-TDL TDC, featuring a TDM encoder, achieves remarkable results, with a minimum measurable pulse width of 520 ps and an average rms precision below 5.3 ps. It sustains a high throughput of 250Msamples/s for arrival time and TOT measurements.
- **Superiority:** Compared to other FPGA-based TOT TDCs, the dual-TDL TDC excels in timing precision and resource efficiency.

TDC Architecture

Dual TDL TDC Stracture

- **Dual TDL Module:** Processes pulse edges separately in TDLs for fine timestamp generation.
- **Trigger and Ripple Generator:** Initiates ripple signals in TDLs for multi-measurements.
- **Clear Logic:** Ensures proper pulse generation and guards against invalid pulses during reset.
- **TDM Encoder:** Converts TDL statuses into fine timestamps, adeptly handling the latched status from dual TDLs.

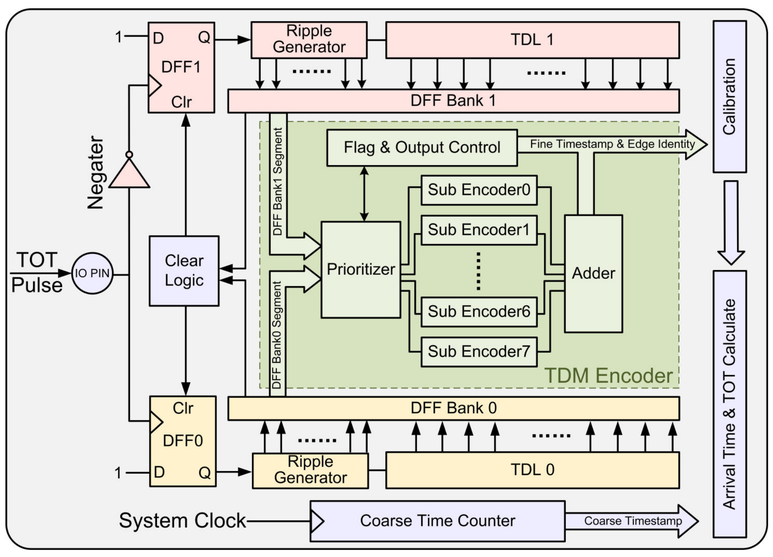
Dual TDL Module

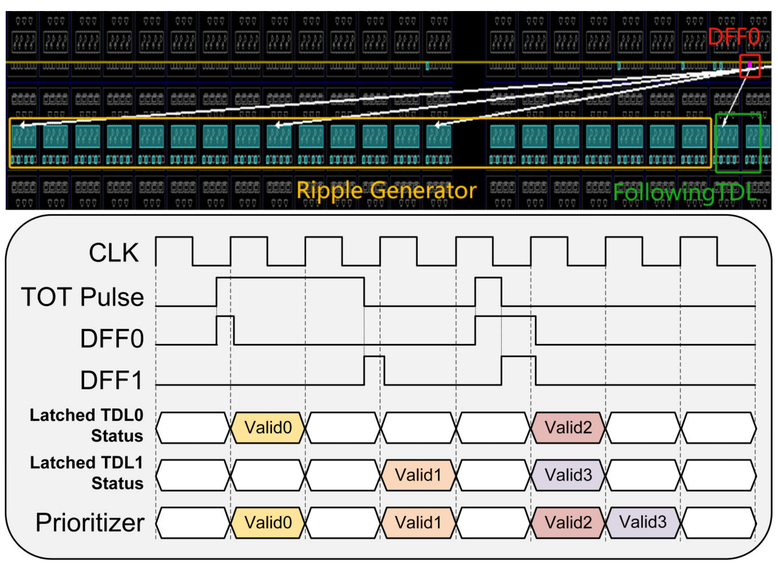
Our design efficiently controls delay sensitivity in the ripple generator by managing the relative locations of DFF0 & TDL0 and DFF1 & TDL1 using Vivado's RLOC Constraints.

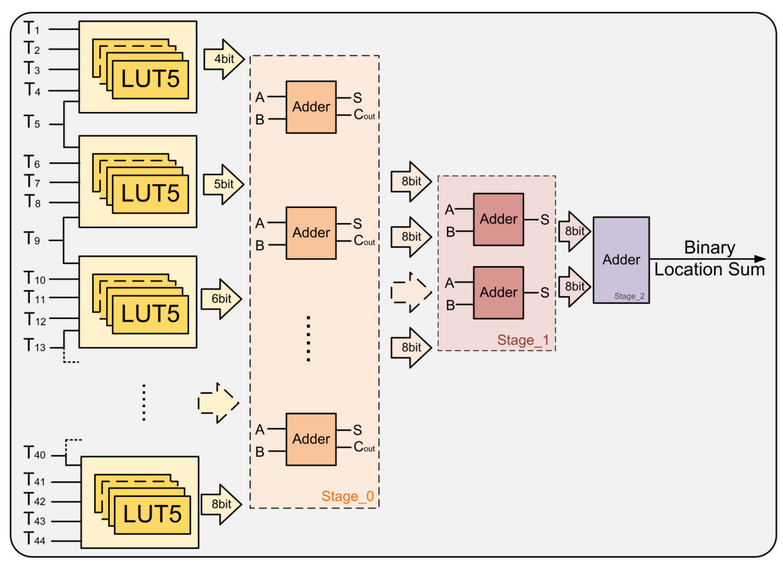
The prioritizer selects between segments from DFF bank0 and DFF bank1 based on activity, ensuring smooth transmission even when both TDLs are active due to narrow pulse widths, preventing data congestion.

TDM Encode Scheme

- **Prioritization:** Selects one valid status from TDL0 or TDL1 based on the clock cycle.
- **Subsequence Decomposition:** Breaks down TDL status into subsequences to identify transition edges.
- **Sub-encoder Construction:** Calculates transition edge positions in 5-bit fragments using LUT5 groups and adders.
- **Aggregation:** Sums binary encoded values from all sub-encoders to represent the TDL status.



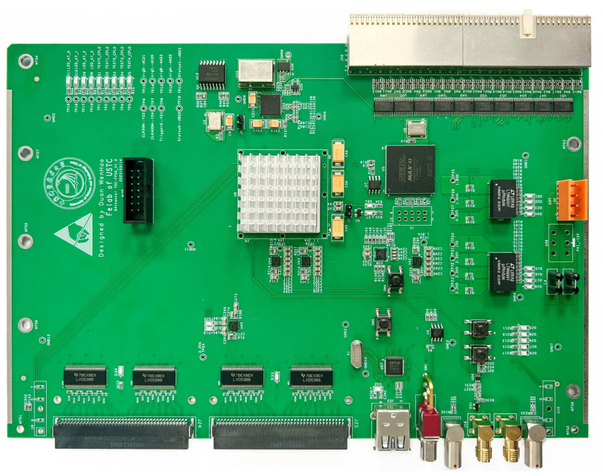




Performance Test

Test Environment

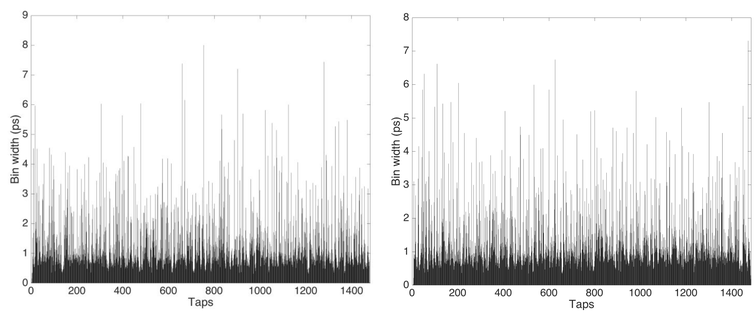
A series of **2, 4, 6, and 8-edge Dual TDL TDCs** were implemented on a custom TDC evaluation board utilizing the **Xilinx xc7k410t-2ffg900i** FPGA.



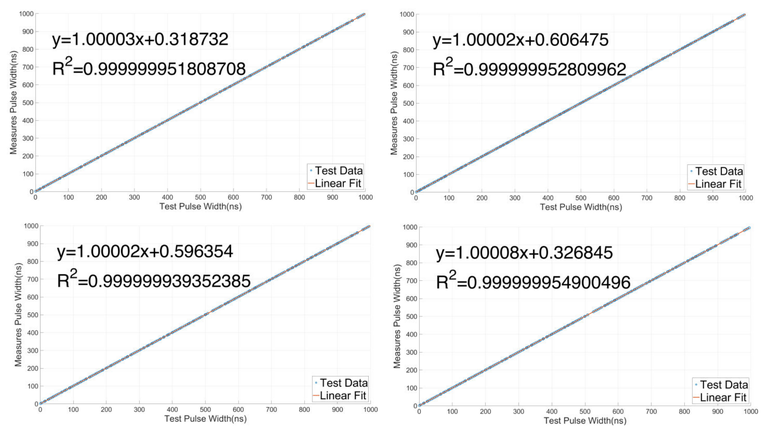
Pulse range from 520 ps to 1000 ns is generated by pulse pattern generator: **Agilent 81134A**.

Calibration

The **code density test** evaluates a Time-to-Digital Converter's performance by analyzing the distribution of measured time intervals, providing crucial insights into resolution and linearity.

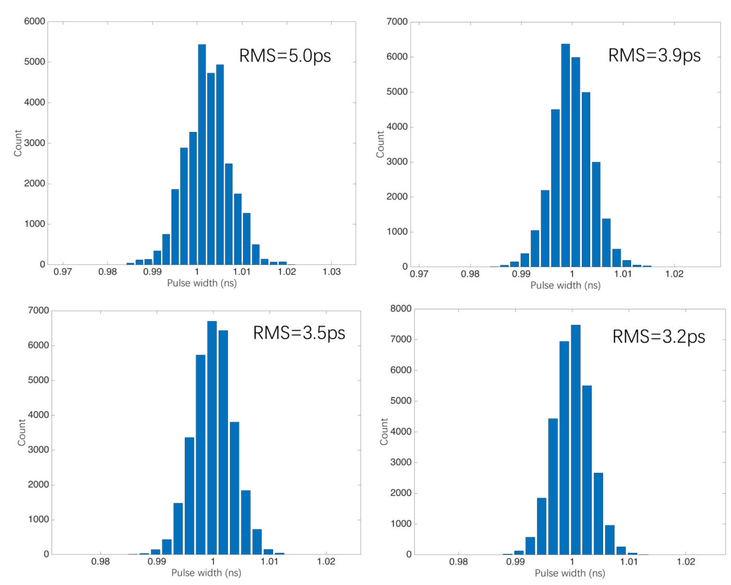


Offset calibration aligns measured pulse edges with actual pulse edges by determining the offset using a linear fit method, enhancing the accuracy of time measurements in TDCs.

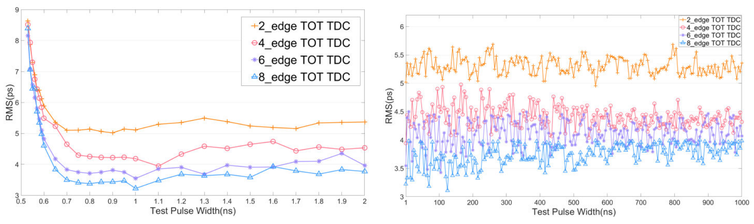


RMS Precision

The precision and dynamic range of 2, 4, 6, and 8-edge Dual TDL TDCs are assessed, revealing typical rms errors of **5 ps, 3.9 ps, 3.5 ps, and 3.2 ps** respectively at 1 ns TOT time.

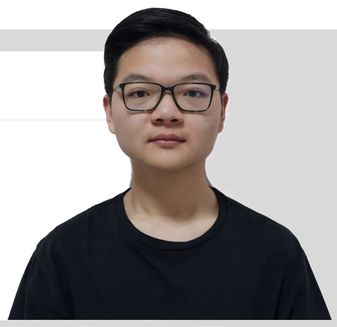


The average rms errors are respectively measured to be **5.3 ps, 4.4 ps, 4.1 ps, and 3.7 ps**.



Conclusion

- Dual TDL TDC provides high precision, high throughput, and narrow pulse width measurement capabilities for TOT measurements.
- Leveraging advanced architecture and multi-edge measurement, Dual TDL TDC offers a dynamic range from 520 ps to 1000 ns, with 250 MSamples/s throughput, ideal for modern physics experiments.



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