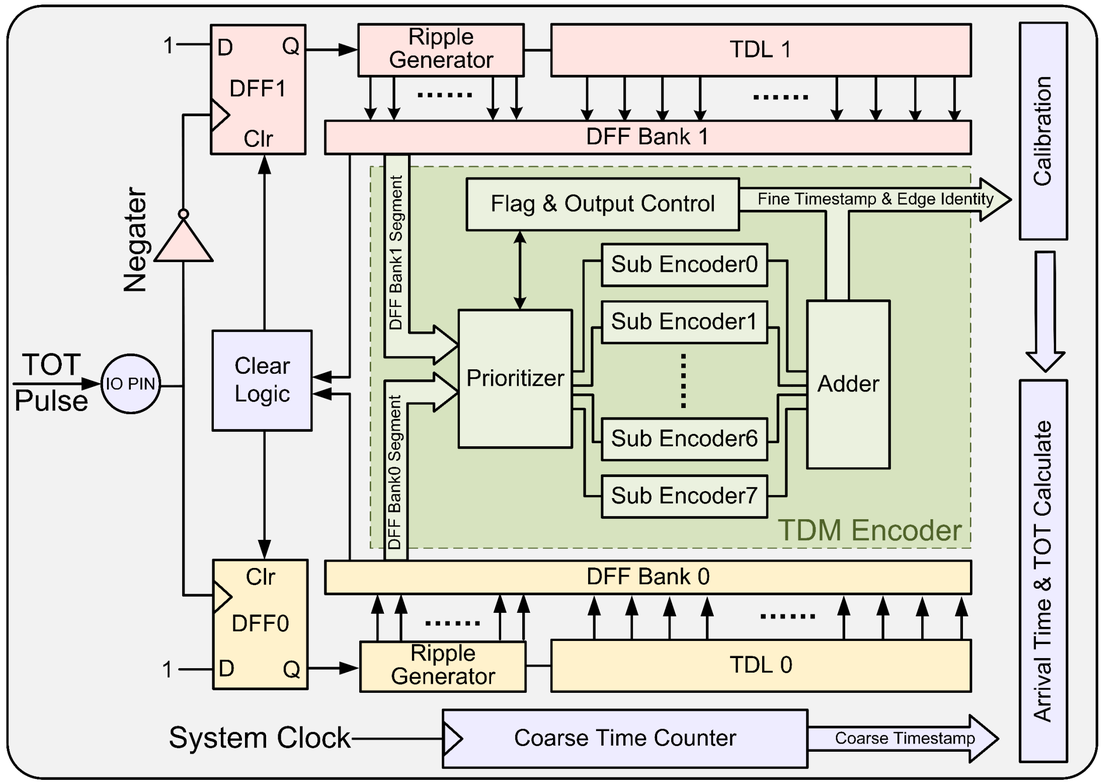
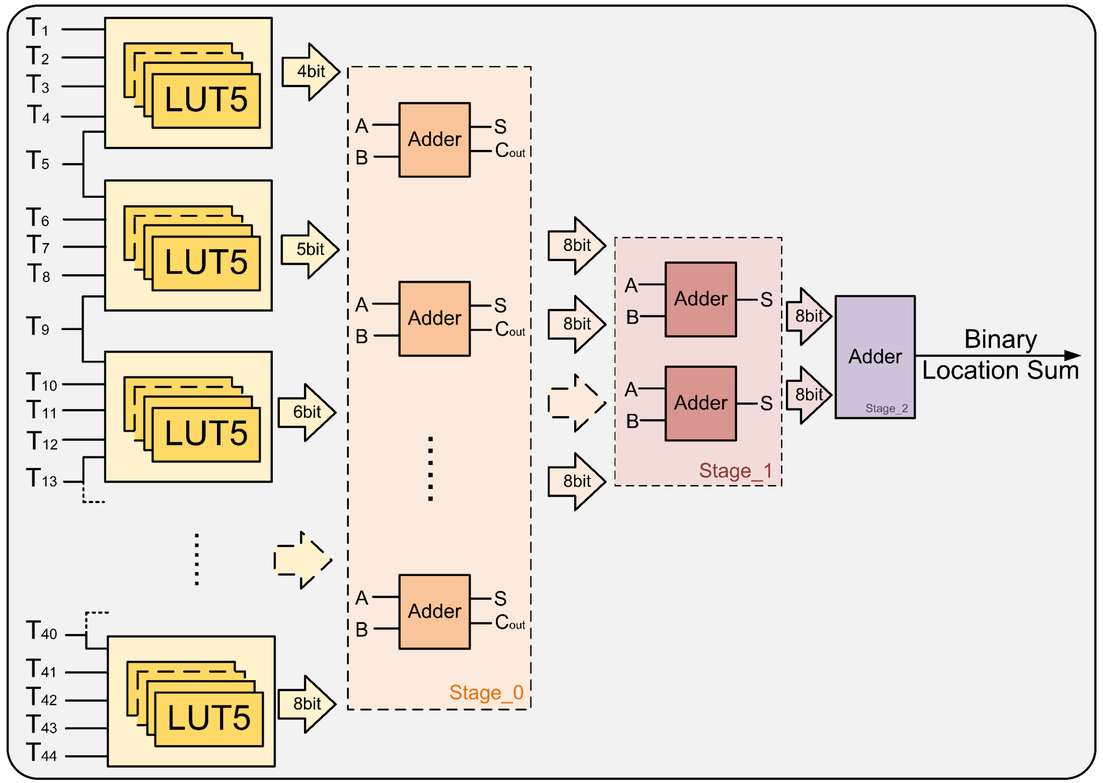
Dual TDL TDC Featuring a TDM Encoder

Dual TDL Structure: Processes pulse edges separately in TDL0 & TDL1 for fine timestamp generation

TDM encoder: Converts TDL statuses into fine timestamps, preventing data congestion

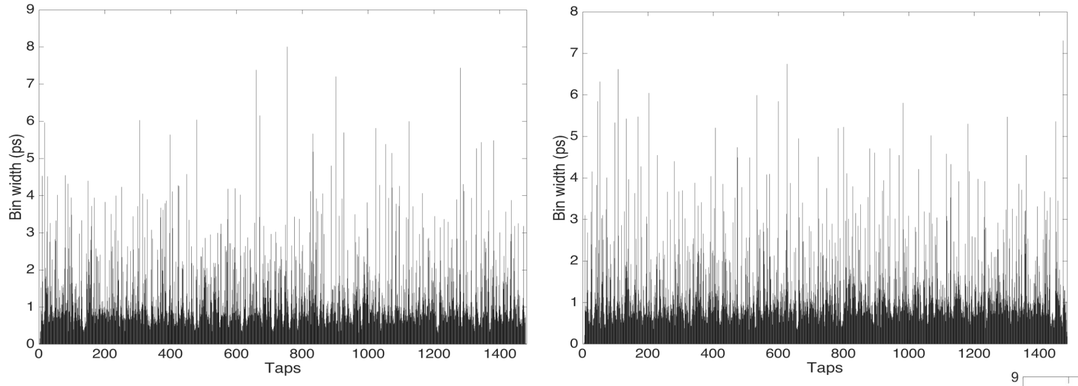




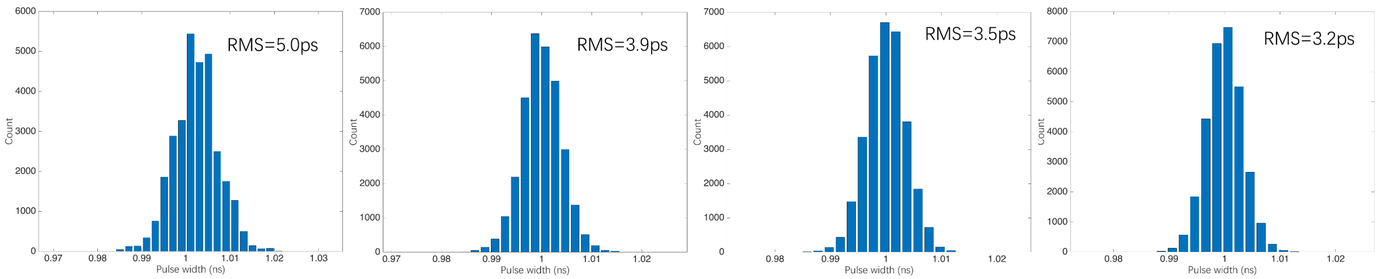
ID #91 “An FPGA-Based High Precision Pulse Width Measurement Time-to-Digital Converter with Time Division Multiplexing Encoder”
Author: **Wenhao Duan**, Changqing Feng*, Junchen Wang, Yu Wang, Zhongtao Shen, Shubin Liu
State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei 230026, China.

Performance Evaluation

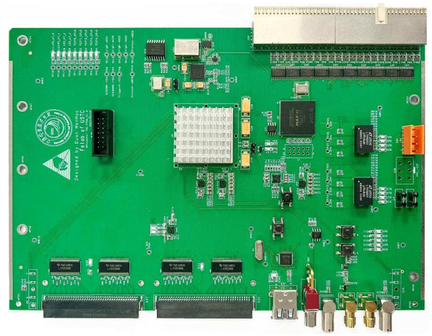
Leveraging advanced architecture and multi-edge measurement, Dual TDL TDC offers a dynamic range from 520 ps to 1000 ns, with 250 MSamples/s throughput, ideal for modern physics experiments.



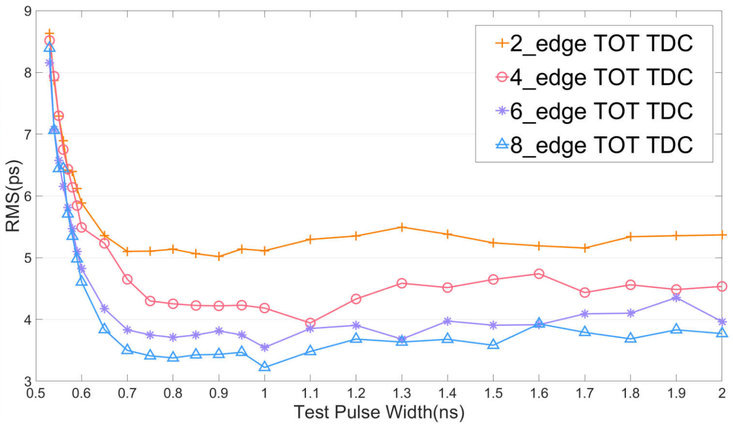
8-edge Dual TDL TDC measured bin width

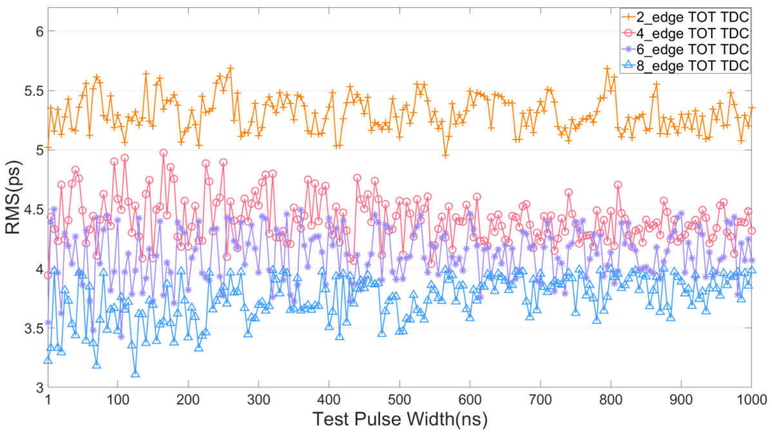


Measured histogram of the TOT time of 1ns



Test Environment





TOT rms errors of the 2, 4, 6, and 8-edge Dual TDL TDCs

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