# A Frequency Division Multiplexing Room-temperature Electronics Readout Scheme for TES Calorimeter Arrays

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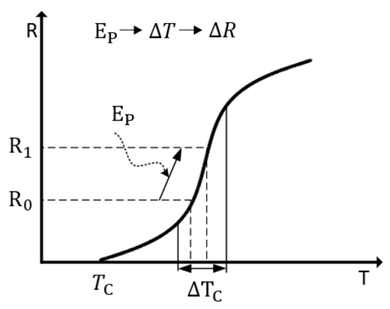
## Introduction

- The Transition-Edge Sensor (TES) is one of the most critical core components of ultra-high-resolution detectors and has broad application prospects
- Owing to the ultra-high temperature sensitivity, large arrays of TES microcalorimeters have been used in space-based and ground-based experiments within the fields of astrophysics and particle physics
- The detector comprises an absorber, a TES-based thermometer, and a thermal bath. When operating as a calorimeter, TES is weakly coupled to a thermal bath at a temperature lower than the TES critical temperature and well coupled to an absorber
- The number of thermal loads that connect the cryogenic calorimeter to the room-temperature electronics must be strictly limited
- It is desirable to multiplex several signals onto a reduced number of wires

## Principle

### TES Principle

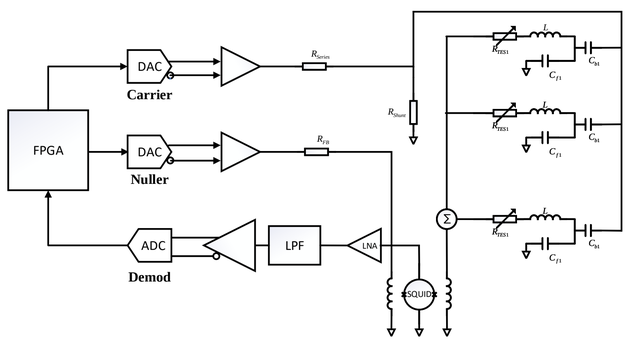
TES is actually a superconducting film that can be self-heated and stably maintained in the transition state by means of an AC or DC bias circuit. Its resistance changes sharply with temperature. When a incident particle with energy $E_p$ is absorbed, the temperature of the absorber will increase by $T = E_p/C_e$. Changes in the TES resistance will cause changes in the branch current. Then the branch current is amplified by superconducting quantum interference devices (SQUID) and processed by the room temperature readout circuit.




### Readout Structure

The readout system consists of three part:

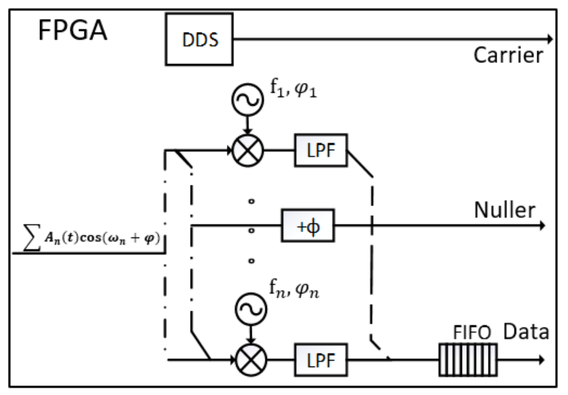
- Demodulator: The LPF consists of a forth-order passive RC low-pass filter and an operational amplifier. The A/D converter (ADC) is a low-noise 18-bit 65 MSPS high-speed ADC.
- Nuller: Signals are generated by 16-bit 50 MSPS D/A converters (DACs).the value of $R_{FB}$ is about 10K ohms.the output accuracy is about 3nA.
- Carrier: The DAC is same as Nuller's.The $R_{series}$ is about several thousand ohms. The shunt resistor is about 100 milliohms.




### Readout Logic

Each signal is mixed with 40 reference waveforms. The frequency and the phase of the reference waveforms can be programmed independently.

In order to obtain accurate amplitude values, the phase width of the direct digital synthesizers (DDSs) that generate the reference waveform needs to be as large as possible
The carrier frequencies are chosen between 1MHz and 5MHz. They are generated directly by DDSs in FPGA. An on-chip RAM is designed to store the hit information.

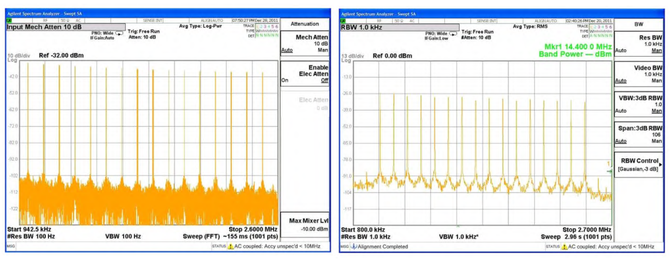



## Design and Test

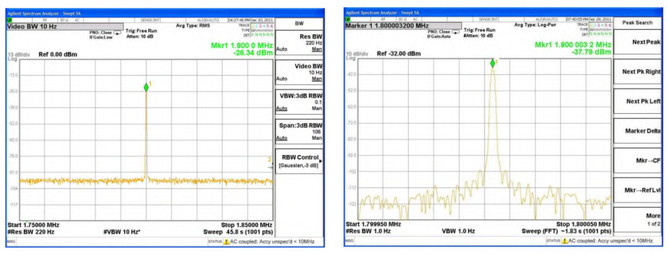
### Bias Test

The DAC generates 16 bias signals, each signal is spaced 0.1MHz apart. Full-scale output and non-full-scale output were tested respectively.

With the help of N9010A EXA signal analyzer, the DAC output signal spectrum diagram was obtained.

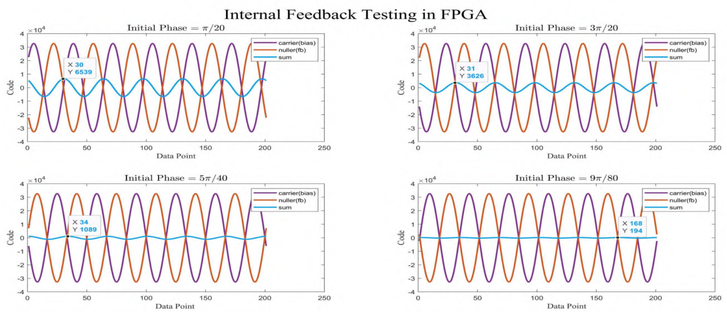


In order to make the test more accurate, we limited the range of the spectrum chart to around 1.8M. The signal-noise ratio (SNR) is about 80dBc.

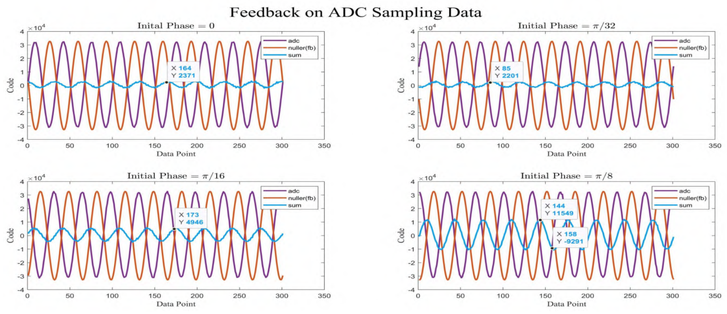


### Nuller Result

By adjusting the phase and amplitude of the nuller signal, a signal inverted with the TES signal is generated at the SQUID input end. When debugging inside the FPGA, the DDS bit width is the same, so only the phase needs to be adjusted.



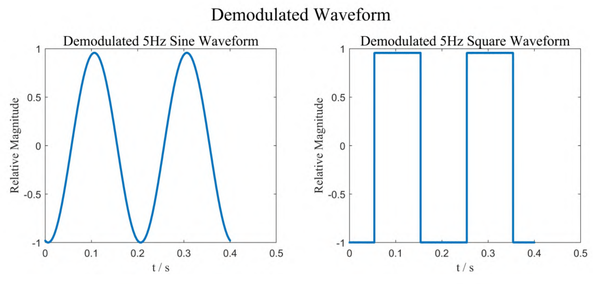

The bias signal and feedback signal are sent to the adder, then they are connected to the ADC. Both the amplitude and phase need to be adjusted.




### Demodulator

By adjusting the phase of the reference waveform, the maximum value obtained represents the amplitude of the input signal at that particular frequency.

Obviously, in order to obtain accurate amplitude values, the phase width of DDSs that generate the reference waveform needs to be as large as possible.




## Conclusion

- The room-temperature electronics function properly. The AD/DA and other chips works well.
- The SNR of Bias signals is about 80 dBc.The logic function of feedback and demodulate is normal.
- Joint debugging testing with TES detectors can be carried out.

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