Study on Readout Electronics of CEPC Scintillator Analog Hadronic Calorimeter Prototype

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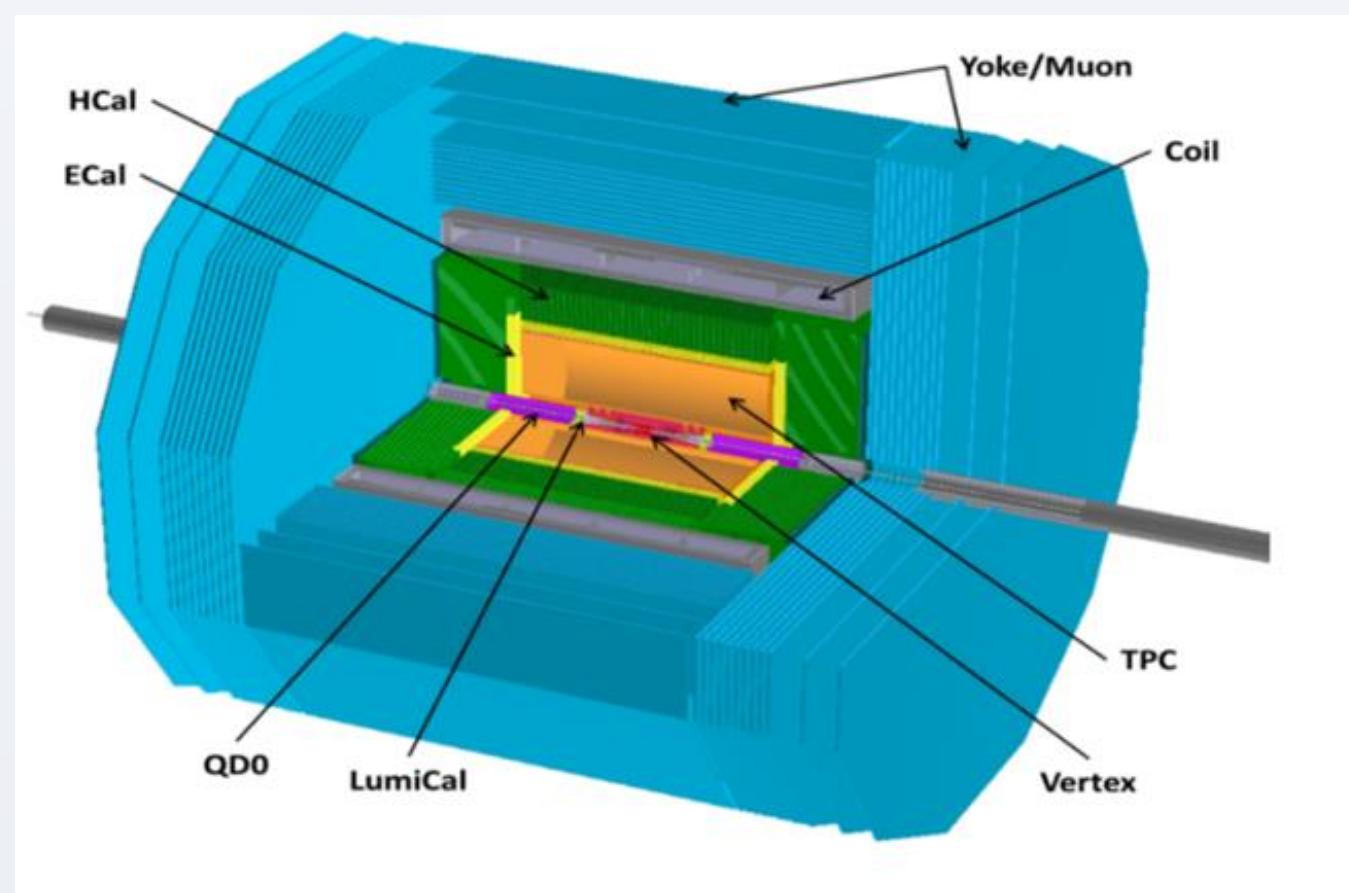
1. Introduction

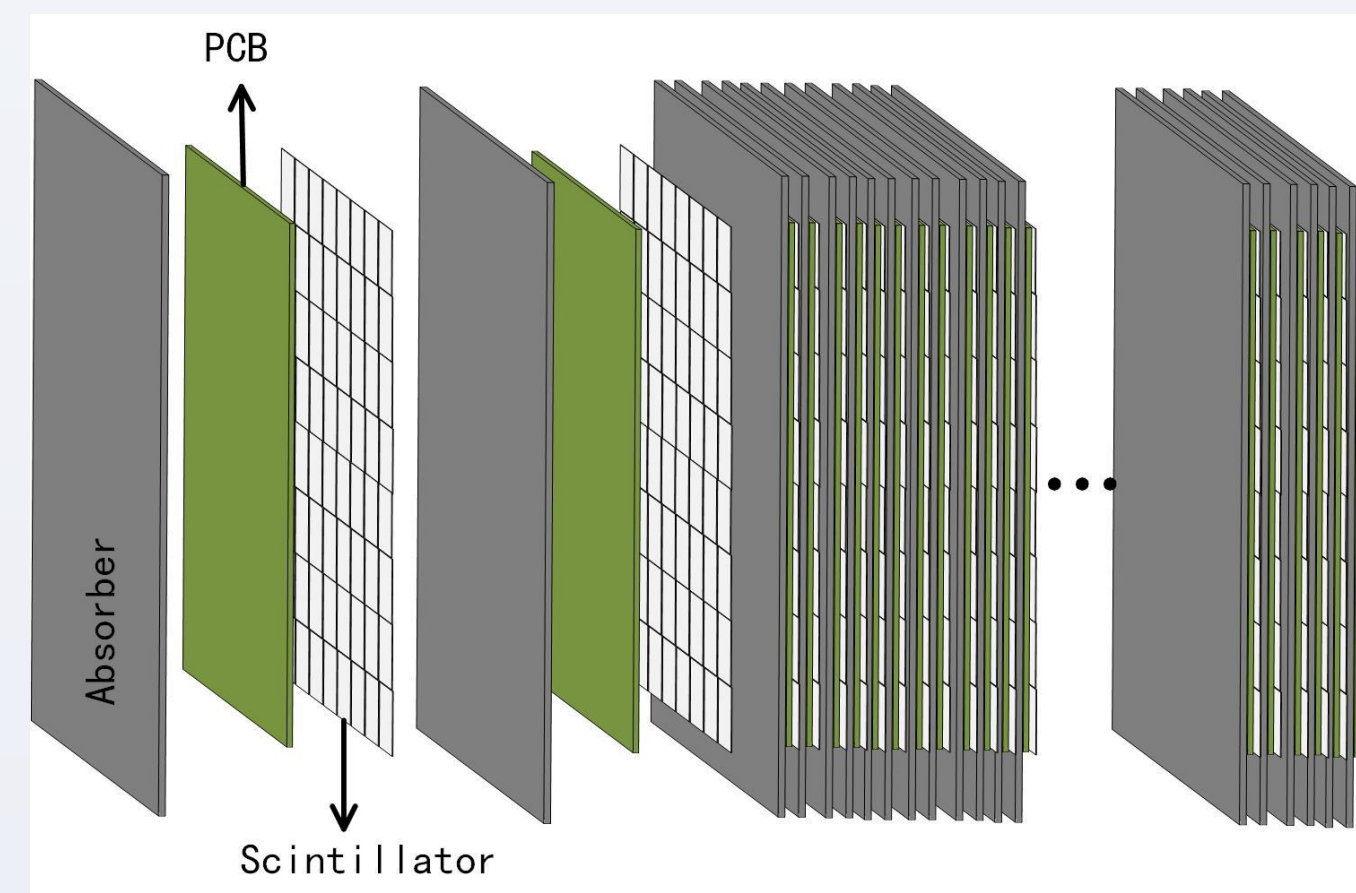Fig. 1 The Structure of CEPC Detector

Fig. 2 The 40-layer Sc-AHCAL prototype

As a Higgs and Z factory, circular electron positron collider (CEPC) has been proposed to precisely measure Higgs and Z bosons and learn their properties. For high-resolution energy measurement, the detector incorporates the particle flow algorithm (PFA) with a precision vertex detector, a time projection chamber, a silicon tracker, a high-granularity electromagnetic calorimeter (ECAL), a high-granularity hadronic calorimeter (HCAL) and a muon detector. The scintillator analog hadronic calorimeter (Sc-AHCAL), which is a kind of PFA HCAL technical routes, has been studied and the readout electronics of its prototype is discussed in this paper.

As shown Fig. 2, the Sc-AHCAL prototype a 40-layer calorimeter and each layer contains an absorber layer and a sampling layer. In the sampling layer, plastic scintillators with the size of 40 mm × 40 mm × 3mm are used as active materials and the area of the sample layer is 720 mm × 720 mm. The light-to-charge conversion is finished by the silicon photomultiplier (SiPM) mounted on the bottom of each scintillator.

2. Requirements

The main function of readout electronics is to measure the signals of SiPMs. According to the Monte-Carlo simulation, the range of energy deposition in one scintillator is $1 - 400$ MIPs and base on testing results, the light yield is 17 p.e./MIP. When the SiPM gain is 3.6×10^5 (S14160-1315 from Hamamatsu), the dynamic range is 980 fC to 500 pC, and the electronics noise should be lower than 980/3 fC.

Besides, some other problems should be put into consideration. Firstly, for the gain of the SiPM highly depends on the temperature, a temperature monitoring and compensation strategy should be adopted in the electronics system. Secondly, the PFA detector has the feature of fine granularity, which raises demands of high integration to the electronics and the total channel number is 12,960. Finally, the system should also have the function of calibrating itself.
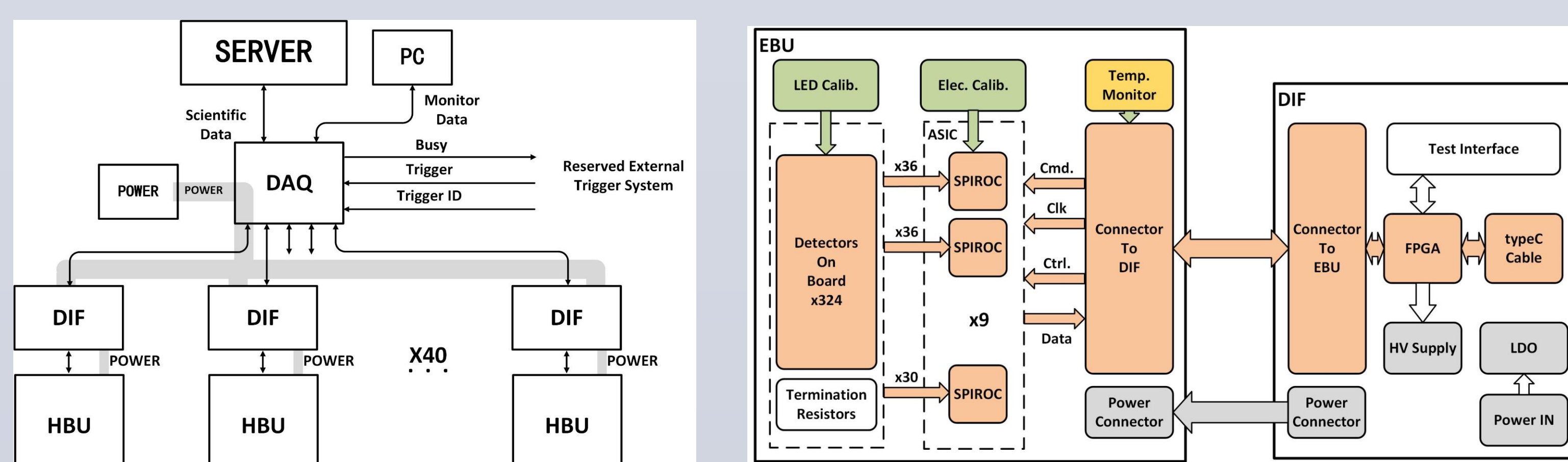
3. Readout System and Modules

Fig. 3 The Structure of Readout System and Single Layer Module

The readout structure of the AHCAL prototype is shown in Fig. 3. The system consists of a data server, a Data Acquisition Board (DAQ), 40 Data Interface Boards (DIF) and 40 HCAL Basic Units (HBU).

One DIF and one HBU are in charge of the signal readouts of one layer. As shown in Fig. 3, there are 9 ASIC chips named SPIROC on an HBU board. SPIROC is a chip specified for SiPMs, which integrates 36 channels in one chip. The DIF board, which is the interface between the HBU and the DAQ, contains a FPGA chip for controlling the HBU and the power circuit for powering up the HBU.

To improve the in integration of the front-end electronics, the readout circuits are mounted on one side of HBU and the SiPMs and the scintillators are mounted on the other side of the board.

4. Challenges and Solutions

To compensate the SiPM gain variation due to temperature, 16 temperature probes are put on every EBU to monitor the environment temperature. The temperature field of HBU can be established based on the probe value so the compensation can be carried out. An experiment is performed to verify the reconstruction of the temperature field and the results shows that the error is less than 0.5 ℃.

Besides, on HBU there is a light calibration circuit for every SiPM which consist of a LED and its drivers. By this circuit, the status of every SiPM can be calibrated and next figure is a single photon spectrum of a SiPM.
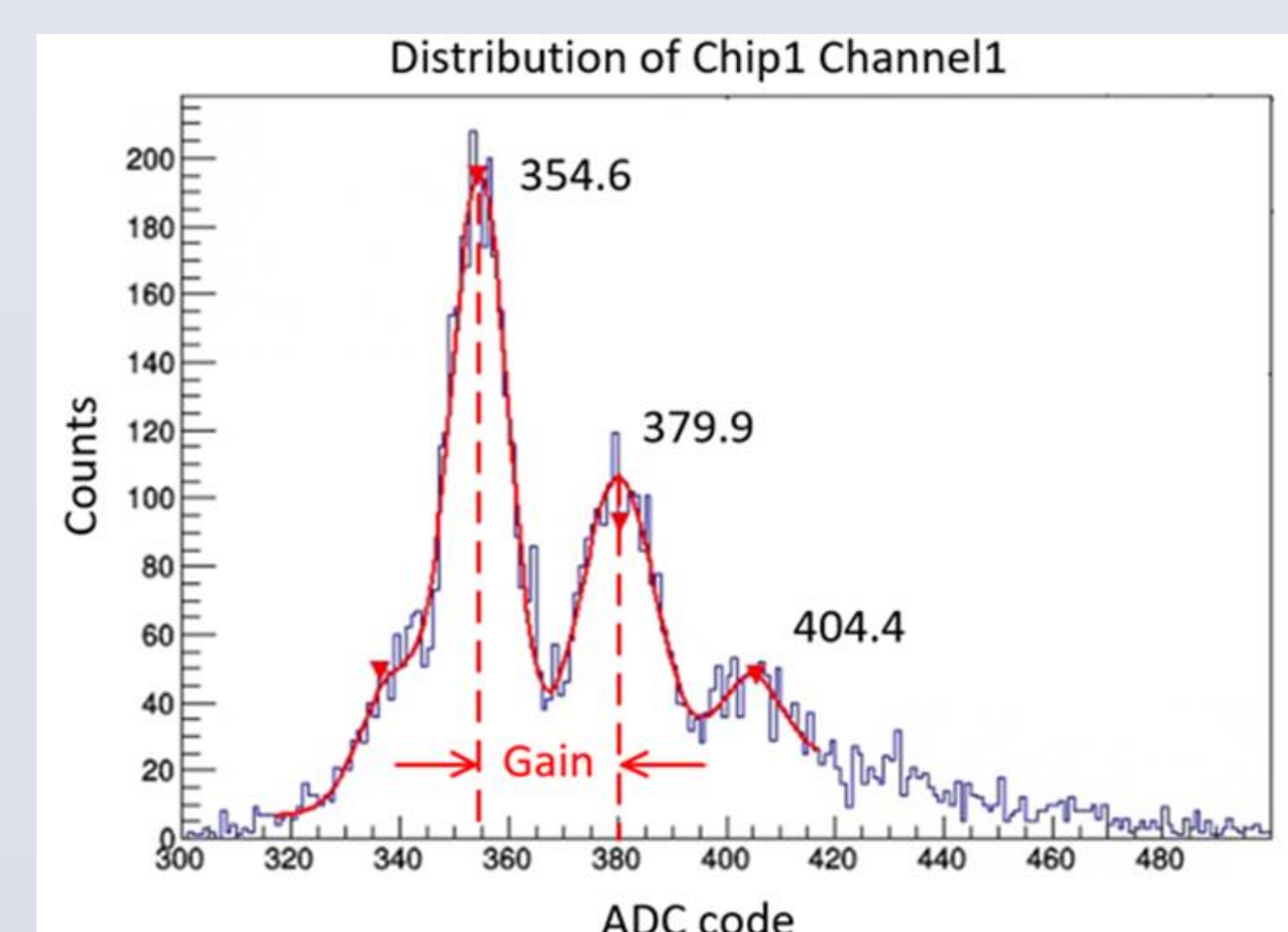

Fig. 4 Single Photon Spectrum

Fig. 5 Photo of AHCAL Prototype

5. Tests and Results

To verify the function of the readout system, a beamtest combined with CEPC Sc-ECAL prototype is carried out. The results prove the system performs well and Fig. 4 is the reconstruction of two beamtest events.
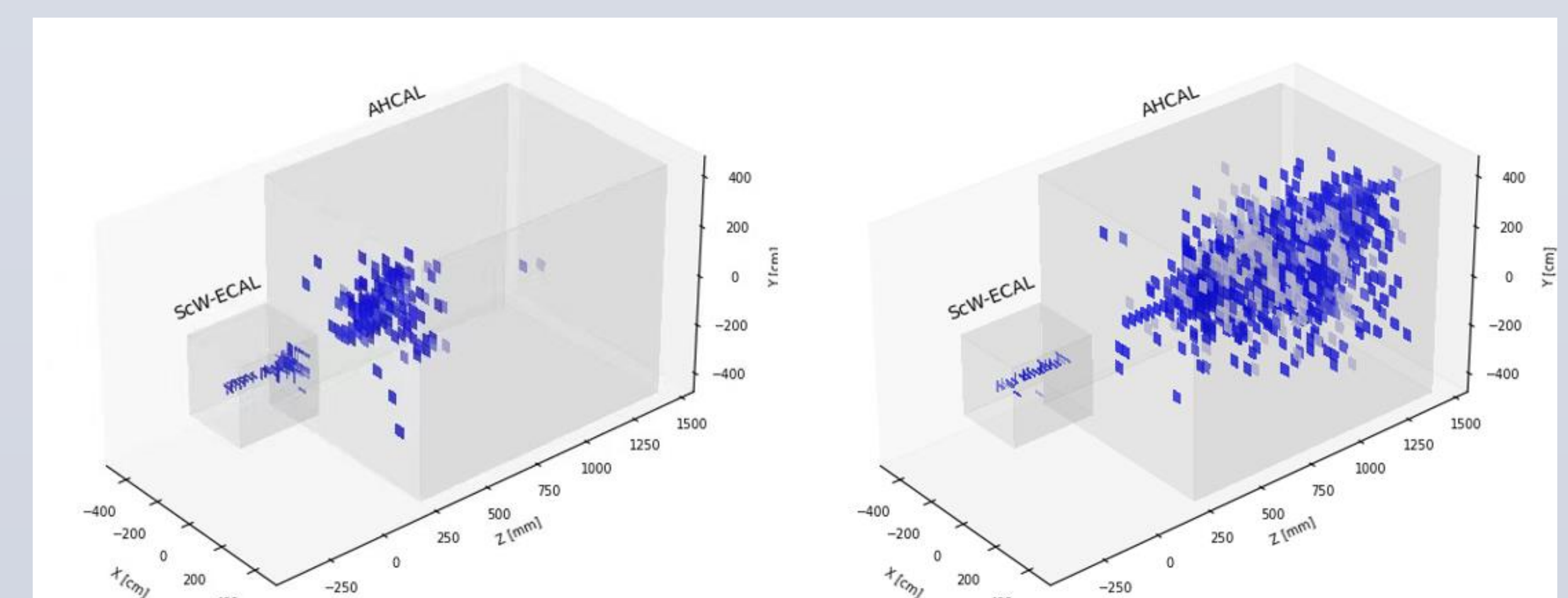

Fig. 4 Reconstruction of Two Beamtest Events.

Acknowledgement