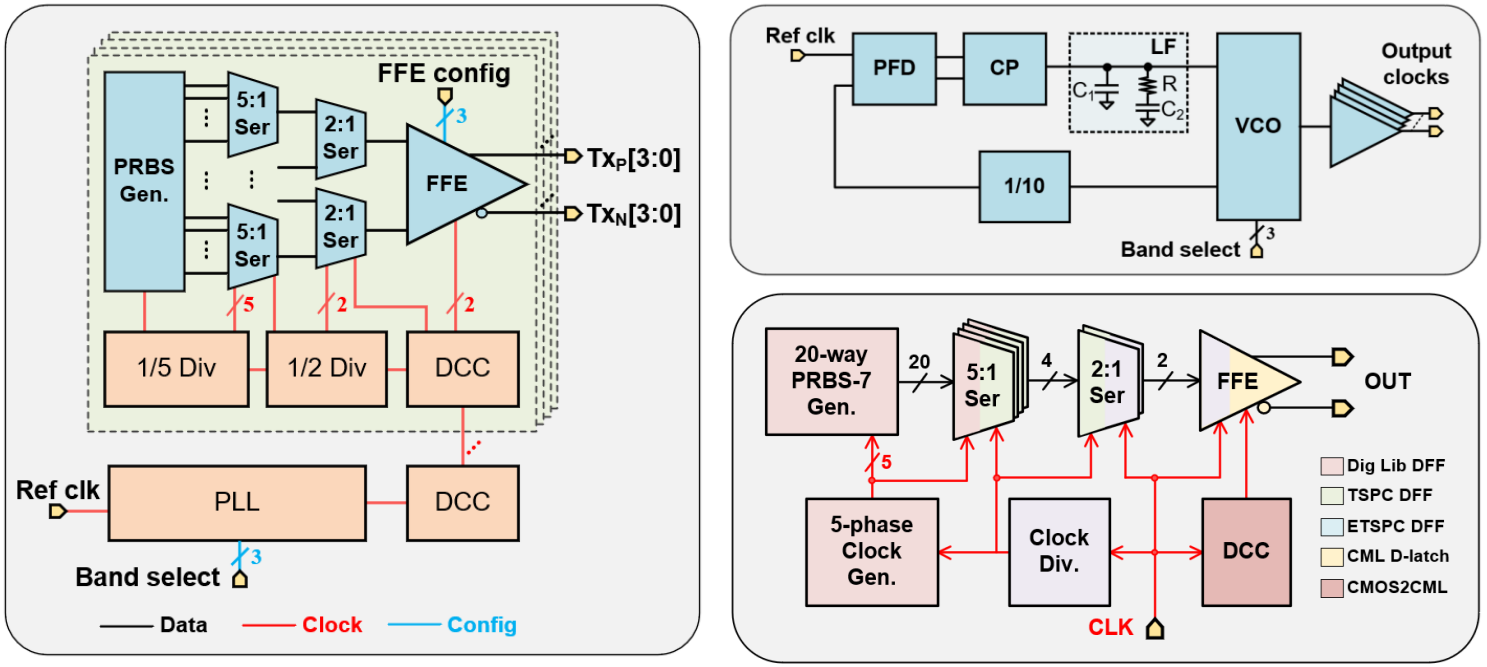
A 4×6.25-Gbps Serial Link Transmitter Core in 0.18-μm CMOS for high-speed front-end ASICs

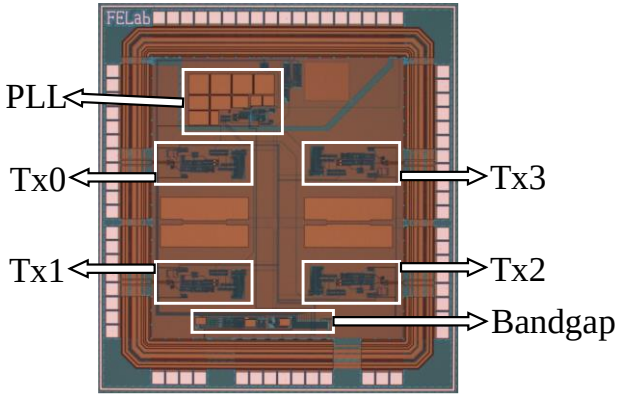
With the increasing luminosity and the trend of digitization forward
more data bandwidth will be needed in front-end ASICs



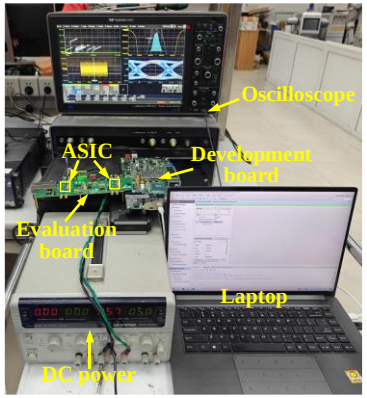
High data bandwidth, Low jitter, Low power consumption
- Differential delay cell based 3-stage VCO
- 3-bit band select to reduce K_{VCO}
- 3-bit adjustable FFE for various channel loss
- 4 types of latch/flip-flops are used according to the operating frequency of each stage

Transmitter Core Performance

A prototype ASIC with embedded PRBS-7 generator has been fabricated and tested.



Micrograph of chip



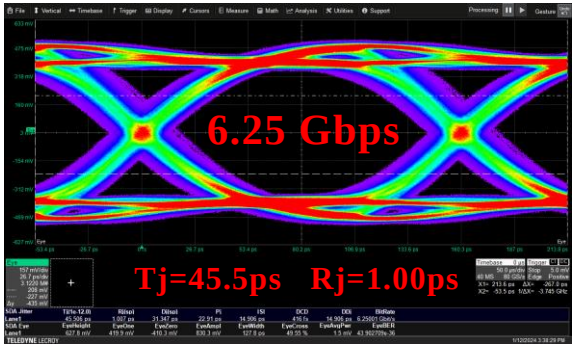
Test platform

Parameter	Value	
Technology	0.18 μm CMOS	
Supply Voltage	1.8 V & 3.3 V	
Data rate	4×6.25 Gbps (3.5~6.75 Gbps)	
Area	PLL	0.12 mm^2
	Transmitter	0.08 mm^2×4
Jitter @6.25 Gbps	PLL	1.006 ps RMS
	Transmitter	45.5 ps @BER=1×10^{-12}
Power @6.25 Gbps	PLL	79 mW
	Transmitter	154 mW×4
	Overall	27.8 mW/Gbps

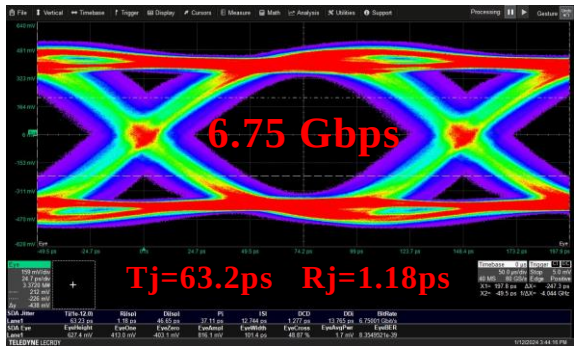
Summary of Performance

The transmitter core operates correctly from 3.5 ~ 6.75 Gbps.

Eye-diagram at 3.5 Gbps



Eye-diagram at 6.25 Gbps



Eye-diagram at 6.75 Gbps

No bit error after 24-hour transmission (about 5.4×10^{14}bit) between ASIC and GTP of AC701.

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